Design of Modulo $2^n-2^k-1$ Adder for Residue Number System

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ABSTRACT

Modular adder is one of the key components for the application of residue number system (RNS). Modulo set with the form of can offer excellent balance among the RNS channels for multi-channels RNS processing. In this paper, a novel algorithm and its VLSI implementation structure are proposed for modulo adder. In the proposed algorithm, parallel prefix operation and carry correction techniques are adopted to eliminate the re-computation of carries. Thus, we can get flexible tradeoff between area and delay with the proposed structure. Compared with same type modular adder with traditional structures, the proposed modulo adder offers better performance in delay and area.

Keywords: Carry correction, modular adder, parallel prefix, residue number system (RNS), VLSI.