Soft Switching Cascaded DC-DC Converter with High Voltage Gain

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ABSTRACT

Increased energy demands and global rising pollution awareness has resulted in significant growth in the field of sustainable energy, hence much of the research work is focused on green power technologies. Renewable energy sources such as photovoltaic (PV) cell and fuel cell are characterized by low voltage and high current output and have strict current ripple requirement. Hence as an important power electronic interface DC-DC converter plays vital role in distributed generation (DG) system/hybrid system to have lower input current ripple and high output DC link voltage. Therefore, in this work, it is aimed to develop a high gain high efficiency DC-DC converter as a power electronic interface for a renewable energy sources. A zero-voltage-switching (ZVS) dc–dc converter with high voltage gain is proposed. It consists of a ZVS boost converter stage and a ZVS half-bridge converter stage and two stages are merged into a single stage. The ZVS boost converter stage provides a continuous input current and ZVS operation of the power switches. The ZVS half-bridge converter stage provides a high voltage gain. The principle of operation and system analysis are presented. Theoretical analysis and performance of the proposed converter were verified on a 100 W experimental prototype operating at 108 kHz switching frequency.

Keywords: Boost converter, coupled inductor, high voltage gain, reverse recovery, zero-voltage switching.

I. INTRODUCTION

Recently, dc–dc converters with steep voltage ratio are usually required in many industrial applications. For example, the front-end stage for clean-energy sources, the dc back-up energy system for an uninterruptible power supply (UPS), high-intensity discharge lamps for automobile headlamps, and, finally, the telecommunications industry [1]–[3]. The conventional boost converters cannot provide such a high dc voltage gain, even for an extreme duty cycle. It also may result in serious reverse-recovery problems and increase the rating of all devices. As a result, the conversion efficiency is degraded and the electromagnetic interference (EMI) problem is severe under this situation [4]. In order to increase the conversion efficiency and voltage gain, many modified boost converter topologies have been investigated in the past decade [5]. In dc–dc converters with high voltage gain, there are several requirements such as high voltage gain, low reverse-recovery loss, soft-switching characteristic, low-voltage stress across the switches, electrical isolation, continuous input current, and high efficiency. In order to meet these requirements, various topologies are introduced. In order to extend the voltage gain, the boost converters with coupled inductors are proposed in [6] and [7]. The voltage gain is extended but continuous input current characteristic is lost and the efficiency is degraded due to hard switching of power switches. In [8], a step-up converter based on a charge pump and coupled

Inductor is suggested. Its voltage gain is around 10 but its efficiency is not high enough due to the switching loss. In [9], a high-step-up converter with coupled inductors is suggested to provide high voltage gain and a continuous input current. However, its operating frequency is limited due to
the hard switching of the switches. In [10], a new boost converter with a ripple free input current was suggested. In the new boost converter, an extra LC circuit with coupled inductors was utilized. The ripple component of the input current was reduced by carefully designing the parameters of the coupled inductor. Coupled inductor can serve as a transformer to extend the voltage gain in non-isolated DC/DC converters. The coupled inductor has two windings. The primary winding serves as the second winding operates as a voltage source in series to the power branch. The voltage gain can be extended by a proper turn ratio design of the coupled inductor. However, the efficiency could not be improved due to the switching losses of the power switch. To increase the efficiency and power conversion density, the soft-switching technique is required in DC/DC converters. In [11]–[16], various soft-switching techniques are suggested. Generally, there is a tradeoff between soft-switching Characteristic and high voltage gain. It is because an inductor that is related with soft-switching limits the voltage gain.

In order to solve these problems, a zero-voltage-switching (ZVS) dc–dc converter with high voltage gain is proposed. As shown in Fig. 1, it consists of a ZVS boost converter stage to make the input current continuous and provide ZVS functions. In Fig. 2 ZVS boost converter and ZVS half-bridge converter stage to provide high voltage gain and continuous input current, soft switching operation. Since single power processing stage can be a more efficient and cost-effective solution, both stages are merged and share power switches to increase the system efficiency and simplify the structure. Since both stages have the ZVS function, ZVS operation of the power switches can be obtained with wider load variation. Moreover, due to the ZVS function of the boost converter stage, the design of the half-bridge converter stage can be focused on high voltage gain. Therefore, high voltage gain is easily obtained. ZVS operation of the power switches reduces the switching loss during the switching transition and improves the overall efficiency. The theoretical analysis is verified by a 100W experimental prototype with 24V-to-86V conversion.

ZVS DC-DC Converters with high voltage gain was proposed in this project which consists of ZVS Boost converter and ZVS Half bridge converter. Analysis of the proposed converter with design parameters are shown below.

II. Analysis of Proposed Converter

A ZVS boost converter with a coupled inductor is proposed. The ZVS characteristic of the proposed boost converter reduces the switching losses and raises the overall efficiency. Moreover, since the ZVS characteristic is achieved by adding an additional winding to the boost inductor, there is only one magnetic component. The reverse-recovery of the auxiliary diode is alleviated due to the leakage inductance of the coupled inductor. The theoretical analysis is verified by a 100W experimental prototype with 24V-to-86V conversion.

The equivalent circuit of the proposed converter is shown in Fig. 2. The ZVS boost converter stage consists of a coupled inductor \( L_c \), the lower switch \( Q_1 \), the upper switch \( Q_2 \), the auxiliary diode \( D_a \), and the dc-link capacitor \( C_{dc} \). The diodes \( D_{Q1} \) and \( D_{Q2} \) represent the intrinsic body diodes of \( Q_1 \) and \( Q_2 \). The capacitors \( C_{Q1} \) and \( C_{Q2} \) are the parasitic output capacitances of \( Q_1 \) and \( Q_2 \). The coupled inductor \( L_c \) is modeled as the magnetizing inductance \( L_{m1} \), the leakage inductance \( L_{k1} \), and the ideal transformer.
that has a turn ratio of 1:n1 (n1 = N1/Np1). The ZVS half-bridge converter stage consists of a transformer T, the switches Q1 and Q2, the output diodes Do1 and Do2, the dc blocking capacitors Cm1 and Cm2, and the output capacitor Co. The transformer T is modeled as the magnetizing inductance Lm2, the leakage inductance Lk2, and the transformer transformer that has a turn ratio of 1:n2 (n2 = N2/Np2). The theoretical waveforms of the proposed converter are shown in Fig. 3. The switches Q1 and Q2 are operated asymmetrically and the duty ratio D is based on the switch Qn. The operation of the proposed converter in one switching period Ts can be divided into seven as shown in Fig. 4. Just before Mode 1, the upper switch Q2, the auxiliary diode Da, and the output diode Do are conducting. The magnetizing current im1 of Lc arrives at its minimum value Iin(m1) and the auxiliary diode current iao arrives at its maximum value Iao. The current i has its maximum value Ia1.

![Fig. 3 Equivalent circuit of the proposed soft-switching dc-dc converter](image)

**Mode 1 [t0, t1]:** At t0, the upper switch Q2 is turned OFF. Then, the capacitor CQ2 starts to be charged and the voltage VQ2 across Q2 increases toward Vdc. Simultaneously, the capacitor CQ1 is discharged and the voltage VQ1 across Q1 decreases toward zero. With an assumption that the output capacitances CQ1 and CQ2 of the switches are very small and all the inductor currents are not changed, the transition time interval T1 can be considered as follows

\[
T_{11} = t_1 - t_0 = \frac{(C_{Q1}+C_{Q2})V_{dc}}{L_{m1} + (n_1 + 1)I_{Da} - I_{m12}}
\]  

(1)

**Mode 2 [t1, t2]:** At t1, the voltage VQ1 across the lower switch Q1 becomes zero and the body diode DQ1 is turned ON. Then, the gate signal for Q1 is applied. Since the current has already flown through the body diode DQ1 and the voltage VQ1 is maintained as zero before the switch Q1 is turned ON, the zero-voltage turn-ON of Q1 is achieved. Since the voltage vP2 across the magnetizing inductance Lm1 is Vin, the magnetizing current im1 increases linearly from its minimum value Iin as follows:

\[
i_{m1}(t) = I_{m12} + \frac{V_{in}}{L_{m1}} (t - t_1)
\]  

(2)

Since the voltage vLk1 across the leakage inductance Lk1 is \(-nV_{in} + V_{dc}\), the auxiliary diode current iao linearly decreases from its maximum value Iao as follows:

\[
i_{ao}(t) = I_{ao} - \frac{nV_{in} + V_{dc}}{L_{k1}} (t - t_1)
\]  

(3)

From (2) and (3), the input current iin is determined as follows:

\[
i_{in}(t) = i_{in}(t) = I_{m12} + \frac{V_{in}}{L_{m1}} (t - t_0) + \frac{nV_{in} + V_{dc}}{L_{k1}} (t - t_0)
\]  

(4)

Since vP2 is \(-V_{dc} - VCB1\) and vLk2 is VCB2+nVvin, the magnetizing current im2 and the diode current iDo1 are given by

\[
i_{m2}(t) = I_{m21} - \frac{V_{dc} - V_{CB1}}{L_{m2}} (t - t_1)
\]  

(5)

\[
i_{Do1}(t) = -i_{CB2}(t) = I_{Do1} - \frac{V_{CB1} + nV_{in}}{L_{k2}} (t - t_1)
\]  

(6)

In this mode, the primary current ip2, the coupled inductor current iL, and the switch current IQ1 can be obtained from

\[
i_{p2}(t) = n_{2}i_{CB2}(t)
\]  

(7)

\[
i_{p}(t) = i_{m2}(t) - i_{p2}(t)
\]  

(8)

\[
i_{Q1}(t) = i_{in}(t) - i_{D0a}(t) - i_{p}(t)
\]  

(9)

**Mode 3 [t2, t3]:** At t2, the current im2 changes its direction. The output diode current iD0a decreases to zero and the diode Do1 is turned OFF. Then the output diode Do2 is turned ON and its current increases linearly. Since the current changing rate of Do1 is controlled by the leakage inductance Lk2 of the transformer T, its reverse-recovery problem is alleviated. Since Vp2 is the same as in Mode 2 and VLB2 is VnVin+VCB2-V0, the current im2 and the diode current iDo2 are given by

\[
i_{m2}(t) = i_{m2}(t) - \frac{V_{in}}{L_{m2}} (t - t_2)
\]  

(10)
$i_{DO2}(t) = i_{CB2}(t) = \frac{V_{CB2} + n_2 V_{in} - V_o}{L_{k2}} (t - t_2)$ (11)

The currents $i_{p2}$, $i_k$, and $i_{Q1}$ can be obtained from the same relations in Mode 2. In this mode, the voltages $V_{P2}$ and $V_{Lk}$ are equal to those in Mode 2. Therefore, the magnetizing current $i_{m1}$, the auxiliary current $i_{Da}$, and the input current $i_n$ change with the same slopes as in Mode 2.

**Mode 4** [I3, t4]: At $t_3$, the auxiliary diode current $i_{Da}$ decreases to zero and the diode $D_a$ is turned OFF. Since the changing rate of the diode current $i_{Da}$ is controlled by the leakage inductance $L_{k}$ of the coupled inductor $L_{c}$, its reverse recovery problem is alleviated. Since the voltage $V_{P1}$ across the magnetizing inductance $L_{m1}$ is the input voltage $V_{in}$, the magnetizing current $i_{m1}$ increases linearly with the same slope as in Modes 2 and 3 as follows:

$$i_{m1}(t) = i_{m1}(t_3) + \frac{V_{in}}{L_{m1}} (t - t_3)$$ (12)

Since the auxiliary diode current $i_{Da}$ is zero, the input current $i_n$ is equal to the magnetizing current $i_{m1}$. At the end of this mode, the magnetizing current $i_{m1}$ arrives at its maximum value $I_{m1}$. Since the voltages $V_{P2}$ and $V_{Lk2}$ are not changed in this mode, the slopes of the current $i_{m2}$, $i_{CB2}$, and $i_k$ are not changed.

**Mode 5** [I4, t5]: At $t_4$, the lower switch Q1 is turned OFF. Then, the capacitor $C_{Q1}$ starts to be charged and the voltage $V_{Q1}$ across Q1 increases toward $V_{dc}$. Simultaneously, the capacitor $C_{Q2}$ is discharged and the voltage $V_{Q2}$ across Q2 decreases towards zero. With the same assumption as in Mode 1, the transition time interval $T_{5}$ can be determined as follows:

$$T_{52} = t_5 - t_4 = \frac{(C_{Q1} + C_{Q2}) V_{dc}}{I_{L2} + I_{m1}}$$ (13)

**Mode 6** [I5, t6]: At $t_5$, the voltage $V_{Q2}$ across the upper switch Q2 becomes zero and the body diode $D_{Q2}$ is turned ON. Then, the gate signal is applied to the switch Q2. Since the current has already flown through the body diode $D_{Q2}$ and the voltage $V_{Q2}$ is maintained as zero before the turn-ON of the switch Q2, the zero-voltage turn-ON of Q2 is achieved. Since the voltage $V_{P1}$ across the magnetizing inductance $L_{m1}$ is $-(V_{dc} - V_{in})$, the magnetizing current $i_{m1}$ decreases linearly from its maximum value $I_{m1}$ as follows:

$$i_{m1}(t) = I_{m1} - \frac{V_{dc} - V_{in}}{L_{m1}} (t - t_5)$$ (14)

Since the voltage $V_{Lk}$ across the leakage inductance $L_k$ is $n_1 (V_{dc} - V_{in})$, the auxiliary diode current $i_{Da}$ linearly increases from zero as follows:

$$i_{Da}(t) = \frac{n_1 (V_{dc} - V_{in})}{L_{m1}} (t - t_5)$$ (15)

From (14) and (15), the input current $i_n$ is determined as

$$i_{n}(t) = I_{n1} - \frac{(V_{dc} - V_{in})}{L_{m1}} (t - t_5) - n_1 \frac{(V_{dc} - V_{in})}{L_{m1}} (t - t_5)$$ (16)

Since the voltage $V_{P2}$ is $V_{CB1} (= D V_{nin})$ and $V_{Lk2} = -(V_o - V_{CB2} + n_2 V_{in} / (1 - D))$, the magnetizing current $i_{m2}$ and the diode current $i_{Da}$ are given by

$$i_{m2}(t) = i_{CB2} + \frac{D V_{in}}{L_{m2} (1 - D)} (t - t_5)$$ (17)

$$i_{Da}(t) = i_{CB2} = \frac{V_o - V_{CB2} + (n_2 V_{in} / (1 - D))}{L_{k2}} (t - t_5)$$ (18)

**Mode 7** [I6, t7]: At $t_6$, the current $i_{CB2}$ changes its direction. The output diode current $i_{m2}$ decreases to zero and the diode $D_{o1}$ is turned OFF. Then the output diode $D_{o2}$ is turned ON and its current increases linearly. Similar to $D_{o1}$, the current changing rate of $D_{o2}$ is controlled by the leakage inductance $L_{o2}$ of the transformer T and its reverse-recovery problem is alleviated. Since $V_{P2}$ is the same as in Mode 6 and $V_{Lk2}$ is $V_{CB2} - n_2 V_{in} / (1 - D)$, the current $i_{m2}$ and the diode current $i_{Da}$ are given by

$$i_{m2}(t) = i_{m2}(t_6) + \frac{D V_{in}}{L_{m2} (1 - D)} (t - t_6)$$ (19)

$$i_{Da}(t) = -i_{CB2} = \frac{V_{CB2} - (n_2 V_{in} / (1 - D))}{L_{k2}} (t - t_6)$$ (20)

The currents $i_{p2}$ and $i_k$ can be obtained from the same relations in Mode 2. In this mode, the voltages $V_{P1}$ and $V_{Lk1}$ are equal to those in Mode 6. Therefore, the magnetizing current $i_{m1}$, the auxiliary current $i_{Da}$, and the input current $i_n$ change with the same slopes as in Mode 2.
Fig. 4 Theoretical waveforms
III. CHARACTERISTIC AND DESIGN PARAMETERS:

1. Voltage Gain of the Boost Converter Stage:
   Referring to the voltage waveform $V_{p1}$ in Fig. 4, the volt second balance law gives
   $V_{in}DT_s - (V_{dc} - V_{in}) (1 - D) T_s = 0. \quad (21)$

   From (21), the voltage gain of the proposed ZVS boost converter stage is obtained by
   $V_{dc} = \frac{1}{1 - D} \quad (22)$
   Which is the same as that of the conventional CCM boost converter.

2. Auxiliary Diode Current Reset Timing Ratio $d_1$:
   By applying the volt-second balance law to the voltage waveform $V_{Lk1}$, the auxiliary diode current reset timing ratio $d_1$ is
   $d_1 = \frac{n_1D(1 - D)}{n_1(1 - D) + 1} \quad (23)$

3. Maximum Auxiliary Diode Current $I_{da}$:
   From Modes 6 and 7, the maximum auxiliary diode current $I_{da}$ is obtained by
   $I_{da} = \frac{n_1DV_{in}T_s}{L_{k1}} \quad (24)$

4. DC-Blocking Capacitor Voltage $V_{CB1}$:
   Referring to the voltage waveform $V_{p2}$ in Fig. 4, the volt second balance law gives
   $V_{CB1} (1 - D) T_s - (V_{dc} - V_{CB1})DT_s = 0 \quad (25)$

   From (22) and (25), the dc-blocking capacitor voltage $V_{CB1}$ is obtained by

   $V_{CB1} = \frac{DV_{in}}{1 - D} \quad (26)$

5. Maximum Output Diode Currents $I_{D01}$ and $I_{D02}$:
   From Modes 2 and 7, the maximum output diode current $I_{D01}$ can be written as follows:
   $I_{D01} = \frac{n_2V_{in} + V_{CB2}}{L_{k2}} - V_{CB2} + \frac{n_2DV_{in}(1 - D)}{L_{k2}} ((1 - D - d_3) T_s \quad (27)$
   $I_{D02} = \frac{n_2V_{in} + V_{CB2} - V_o}{L_{k2}} (D - d_2) \quad (28)$

   $T_s = V_o - V_{CB2} + \frac{n_2DV_{in}(1 - D)}{L_{k2}} d_3 T_s \quad (29)$

6. Output Voltage $V_o$ of the Half-Bridge Converter Stage:
   From (27) and (29), the dc-blocking capacitor voltage $V_{CB2}$ and the output voltage $V_o$ can be derived as follows:
   $V_{CB2} = \frac{D - d_2 - (D/(1 - D)) d_3}{1 - D + d_2 - d_3} n_2V_{in} \quad (30)$
   $V_o = \frac{D - d_2 - (D/(1 - D)) d_3}{(D - d_2 + d_3) (1 - D + d_2 - d_3)} n_2V_{in} \quad (31)$

7. Output Diode Current Reset Timing Ratios $d_2$ and $d_3$:
   Since the average value of the current $i_{CB2}$ should be zero, the following relation can be obtained:
   $(1 - D + d_2 - d_3) I_{D01} = (D - d_2 + d_3) I_{D02} \quad (32)$

   From (27) to (32), the relation between $d_2$ and $d_3$ is obtained by
   $\frac{d_2}{d_3} = \frac{D}{1 - D} \quad (33)$

   Since the average value of the current $i_{CB2}$ is zero, its peak values $I_{m21}$ and $I_{m22}$ have the same value as follows:
   $I_{m21} = I_{m22} = \frac{DV_{in}T_s}{2L_{m2}} \quad (34)$

   From Fig.4, the output current $I_o$ can be represented by
   $I_o = (1 - D + d_2 - d_3) I_{m01} \quad (D - d_2 + d_3) I_{m02} \quad (35)$

   From (27), (28), (33), and (37), $d_2$ and $d_3$ are obtained by
\[
d_2 = \alpha D \\
d_3 = \alpha(1 - D) \\
\alpha = 1/2 \left( 1 - \sqrt{1 - \frac{8Lk_1I_o}{n_2V_{in}DT_s}} \right)
\]

8. Voltage Gain M of the Proposed DC–DC Converter:
From (22), (31), (36), and (37), the voltage gain M of the proposed converter is given by
\[
M = \frac{V_o}{V_{in}} = \frac{n_2D(1 - 2\alpha)}{(D(1 - 2\alpha) + \alpha)(1 - \alpha - (1 - 2\alpha)D)}
\]

9. Input Current Ripple:
The input current ripple \( \Delta i_{in} \) can be written by
\[
\Delta i_{in} = I_{m11} - I_{m12} + n_1I_{Da} = \frac{n_1^2L_{m1} + L_{k1}}{L_{m1}L_{k1}}DV_{in}T_s
\]
To reduce the input current ripple below a specific value \( I^* \), the magnetizing inductance \( L_{m1} \) should satisfy the following condition:
\[
L_{m1} > \frac{1}{(I^*/DV_{in}T_s) - (n_1^2/L_{k1})}
\]

10. ZVS Conditions:
As is seen in Fig. 3, both the boost converter stage and the half-bridge converter stage have ZVS function. From Fig. 3, the ZVS condition for \( Q_2 \) is given by
\[
I_{m11} + I_{m2} = I_{m11} + I_{m22} + n_2I_{Da} > 0. \quad (42)
\]
Since the current values \( I_{m11}, I_{m22}, \) and \( IDa2 \) have positive values, the ZVS condition for \( Q_2 \) is always satisfied. Similarly, for ZVS of \( Q_1 \), the following condition should be satisfied:
\[
I_{m21} + n_2IDa1 + (n_1 + 1) IDa - I_{m12} > 0 \quad (43)
\]
The terms \( I_{m21} \) and \( n_2IDa1 \) are from the half-bridge converter stage and the terms \( (n_1 + 1)IDa \) and \( I_{m12} \) are from the boost converter stage. If the boost converter stage is designed to satisfy the above inequality (43) regardless of the status of the half bridge converter stage, ZVS of the proposed converter is always accomplished. In this case, the leakage inductance \( L_{k1} \) of the coupled inductor \( L_c \) should satisfy the following condition
\[
L_{k1} < \frac{(n_1 + 1) n_1DV_{in}T_s}{P_o/V_{in}} \quad (44)
\]
IV. EXPERIMENTAL RESULTS

A 100W prototype of the proposed converter is made and tested. The power circuit setup is shown in Fig 4.1. Various parameters used in designing the power circuit are as shown the Table 1 Specifications of prototype.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>100W</td>
</tr>
<tr>
<td>Vin</td>
<td>24V</td>
</tr>
<tr>
<td>Vout</td>
<td>396V</td>
</tr>
<tr>
<td>Coupled inductor (Lc) Lm1 / Llk1</td>
<td>800µH / 16.75µH</td>
</tr>
<tr>
<td>Transformer (T) Lm2 / Llk2</td>
<td>474µH / 170µH</td>
</tr>
<tr>
<td>Cdc (Electrolytic capacitor)</td>
<td>470µF/100V</td>
</tr>
<tr>
<td>Inductor Core for coupled inductor (Lc)</td>
<td>ETD49</td>
</tr>
<tr>
<td>Inductor Core for transformer (T)</td>
<td>ETD44</td>
</tr>
<tr>
<td>N1, N2 (Lc)</td>
<td>90,45 turns</td>
</tr>
<tr>
<td>N1, N2 (T)</td>
<td>22,132 turns</td>
</tr>
<tr>
<td>Di, Ds2</td>
<td>MUR460(2)</td>
</tr>
<tr>
<td>Ci</td>
<td>6.6µF</td>
</tr>
<tr>
<td>Cn2</td>
<td>2.2µF</td>
</tr>
<tr>
<td>Co Electrolytic capacitor</td>
<td>220µF</td>
</tr>
<tr>
<td>Q1, Q2</td>
<td>IRF640N</td>
</tr>
<tr>
<td>Da</td>
<td>MUR460</td>
</tr>
</tbody>
</table>
The power is tested in laboratory with the diode bridge rectifier output as input to the converter. Power to control circuit is given from regulated power supply. The waveforms are captured from the oscilloscope and the results are shown in the following section.

V. CONCLUSION

A ZVS dc–dc converter with high voltage gain was suggested. It can achieve ZVS turn-ON of two power switches while maintaining CCM. In addition, the reverse-recovery characteristics of the output diodes were significantly improved by controlling the current changing rate with the use of the leakage inductance of the transformer. The proposed converter presents a higher efficiency and a wider ZVS region compared to other soft-switching converters due to the ZVS boost converter stage. Therefore, the proposed ZVS boost converter is suitable for industrial applications that require a step-up function and a continuous input current characteristic.

REFERENCES


