A ZVS Dual-Input Converter With Hybrid Power Sources

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ABSTRACT

The aim of this study is to develop a high-efficiency converter with two input power sources for a distributed power generation mechanism. The proposed converter can boost the varied voltages of different power sources in the sense of hybrid power supply to a stable output dc voltage for the load demand. An auxiliary circuit in the proposed converter is employed for achieving turn-ON zero-voltage switching (ZVS) of all switches. According to various situations, the operational states of the proposed converter can be divided into two states including a single power supply and a dual power supply. In the dual power-supply state, the input circuits connected in series together with the designed pulse width modulation can greatly reduce the conduction loss of the switches. In addition, the effectiveness of the designed circuit topology and the ZVS properties are verified by experimental results, and the goal of high-efficiency conversion can be obtained.

Key Words: DC–DC converter, hybrid power supply, high-efficiency power conversion, zero-voltage switching (ZVS).

I. INTRODUCTION

In order to protect the natural environment on the earth, the development of clean energy [1]–[3] without pollution has the major representative role in the last decade. By accompanying the permission of Kyoto Protocol, clean energies, such as fuel cell (FC), photovoltaic (PV), wind energy, etc., have been rapidly promoted. Due to the electric characteristics of clean energies, the generated power is critically affected by the climate or has slow transient responses, and the output voltage is easily influenced by load variations. [4]. Thus, a storage element is necessary to ensure proper operation of clean energies. Batteries or super capacitors are usually taken as storage mechanisms for smoothing output power, start-up transition, and various load conditions [5], [6]. The corresponding installed capacity of clean energies can be further reduced to save the cost of system purchasing and power supply. For these reasons, hybrid power conversion systems (PCS) have become one of interesting research topics for engineers and scientists at present.

Based on power electronics technique, the diversely developed power conditioners including dc–dc converters and dc–ac inverters are essential components for clean-energy applications. Generally, one power source needs a dc–dc converter either for raising the input voltage to a certain band or for regulating the input voltage to a constant dc-bus voltage. However, conventional converter structures have the disadvantages of large size, complex topology, and expensive cost. In order to simplify circuit topology, improve system performance, and reduce manufacturing cost, multi-input converters have received more attentions in recent years.

The method for synthesizing multi-input converters was inspired by adding an extra pulsating voltage or a current source to a converter with an appropriate connection. Wai et al. [11], [12] presented multi-input converters with high step-up ratios, and the goal of high-efficiency conversion was obtained. However, these topologies are not economic for the non isolated applications because of the complexity with numbers of electrical components. Tao et al. [13] and Matsuo et al. [14] utilized multi winding-type transformers to
accomplish the power conversion target of multi-input sources. Although these topologies were designed based on time-sharing concept, the complexity of driving circuits will be increased by the control techniques in [13] and [14]. Marchesoni and Vacca [15] investigated a newly designed converter with the series-connected input circuits to achieve the goal of multiple input power sources. The installation cost of the converter with few components was certainly reduced. The feature of [15] is that the conduction losses of switches can be greatly reduced, especially in the dual power supply state. Unfortunately, the hard-switching problem and the huge reverse-recovery current within the output diode degrade the conversion efficiency as a traditional boost converter [6]. Kwasinski [16] discussed the evolution of multiple input converters from their respective single-input versions. Based on several assumptions, restrictions, and conditions, these analyses indicate some feasible and unfeasible frameworks for multiple input developments. Li et al. [17] investigated a set of basic rules for generating multiple-input converter topologies, and systematically generated two families of multiple-input converters. Qian et al. [18] designed a novel converter topology with four power ports including two sources, one bidirectional storage port, and one isolated load port. The zero-voltage switching (ZVS) can be achieved for four main switches. In this study, a high-efficiency ZVS dual-input converter is investigated, and this converter directly utilizes the current source type applying to both input power sources. Based on the series-connected input circuits and the designed pulse width modulation (PWM) driving signals, the conduction loss of the switches can be greatly reduced in the dual power-supply state. Lee et al. [19] performed zero-current-transition dc–dc converters without additional current stress and conduction loss on the main switch during the resonance period of the auxiliary cell. The auxiliary cell provides zero-current-switching turn-OFF for all active switches and minimizes the reverse recovery problem of the main diode. The modified type of this representative auxiliary cell in [19] is introduced into the proposed dual-input converter to reduce the reverse-recovery currents of the diodes.

An auxiliary circuit with a small inductor operated in the discontinuous conduction mode (DCM) is utilized for achieving turn-ON ZVS of all the switches, and the huge reverse-recovery current of the output diode in the traditional boost converter can be removed via the utilization of an auxiliary inductor series connected with a diode. Consequently, the proposed dual-input converter can efficiently convert two power sources with different voltages to a stable dc-bus voltage. According to the power dispatch, this converter could be operated at two states including a single power-supply state and a dual power-supply state. This study is organized into four sections. Following the introduction in Section I, the topology and operation of the proposed high-efficiency dual-input converter are presented in Section II. In Section III, experimental results are provided to validate the effectiveness of the proposed converter. Conclusions are drawn in Section IV.

II. TOPOLOGY AND OPERATION OF DUAL-INPUT CONVERTER

Fig. 1 shows the circuit topology of the proposed ZVS dual-input converter. It contains four parts including a primary input circuit, a secondary input circuit, an auxiliary circuit, and an output circuit. The major symbol representations are summarized as follows. V1 and I1 denote the primary input voltage and current, respectively. V2 and I2 exhibit the secondary input voltage and current, respectively. SP1, SP2, TP1, and TP2 express the power ON/OFF switches and their driving signals produced by the power management. C1, L1, Si, and Ti (i = 1, 2) represent individual capacitors, inductors, switches, and driving signals in the primary and secondary input circuit, respectively. Caux, Laux, Da1, and Da2 are the auxiliary capacitor, inductor, and diodes.
of the auxiliary circuit. \( S_a \) and \( T_a \) are the auxiliary switch and its driving signal, which is generated by the PWM. \( C_o \), \( V_o \), \( I_o \), and \( R_o \) describe the output capacitor, voltage, current, and equivalent load, respectively. For the convenience of analyses, the simplified equivalent circuit is depicted in Fig. 2, and the directional definition of significant voltages and currents are labeled in this figure. The simplification in Fig. 2 is compliant with the following assumptions:

1) all power switches and diodes have ideal characteristics without considering voltage drops when these devices are conducted;
2) the capacitors \( C_a \) and \( C_o \) are large enough so that the voltage ripples due to switching are negligible and could be taken as constant voltage sources \( V_a \) and \( V_o \); and
3) the power ON/OFF switches \( S P_1 \) and \( S P_2 \) are omitted. According to different power conditions, the operational states of the proposed converter can be divided into two states including a single power-supply state with only one input power source and a dual power-supply state with two input power sources.

The powers produced by the voltage sources \( V_1 \) and \( V_2 \) are referred as \( P_1 \) and \( P_2 \), respectively, while the power consumed by the load is referred as \( P_o \). If the condition of \( P_1 > P_o \) (\( P_2 > P_o \)) holds, the switch \( S P_1 \) (\( S P_2 \)) turns ON to supply the power with a single input power source \( V_1 \) (\( V_2 \)). On the contrary, the switches \( S P_1 \) and \( S P_2 \) turn ON to supply the power with two input power sources if the conditions of \( P_1 > P_o \) and \( P_2 > P_o \) fail. The detailed operational stages are described as follows.

\section*{A. Single Power-Supply State}

By turning off one power ON/OFF switch \( S P_1 \) or \( S P_2 \) for cutting off the connection between the power source and the converter, the other input power source \( V_2 \) or \( V_1 \) can supply alone for supporting the output demand. The primary input power supply is considered, for example, to explain how to operate in this state, i.e., the switch \( S P_2 \) is always turned OFF and the switch \( S_2 \) is triggered all the while for minimizing the conduction loss. The switching period is defined as \( T_S \). \( d_1 \) and \( d_2 \) denote the duty cycles of the switch \( S_1 \) and \( S_a \), respectively. \( d_d \) and \( d_{dc} \) present the duty cycles of the dead time and the freewheeling time of the auxiliary inductor. Note that the auxiliary inductor is designed to operate in the DCM. The characteristic waveforms and topological modes of the single power-supply state are depicted in Figs. 3 and 4, respectively. The complete operation modes in a switching period of the converter are discussed as follows.

\begin{itemize}
  \item Mode 1 \([t_0 \rightarrow t_1]\): At \( t_0 \), the auxiliary inductor current \( i_L \) returned to zero. The switch \( S_1 \) is continuously conducted and the auxiliary switch \( S_a \) is still turned OFF. The primary inductor \( L_1 \) is linearly charged by the primary input voltage \( V_1 \). The auxiliary switch voltage \( v_{Sa} \) is equal to the auxiliary capacitor voltage \( V_a \).
  \item Mode 2 \([t_1 \rightarrow t_2]\): At \( t_1 \), the switch \( S_1 \) is turned OFF, the switch voltage \( v_{S1} \) is rising to the auxiliary capacitor voltage \( V_a \), and the auxiliary switch voltage \( v_{Sa} \) is decreasing to zero. The body diode of the auxiliary switch \( S_a \) is conducted for receiving the
\end{itemize}
primary inductor current iL1 to charge the auxiliary capacitor. Therefore, the switch current iSa is negative. Besides, the auxiliary inductor current linearly increases, and its slope is dependent on the auxiliary inductor voltage vLa, which is equal to Va – Vo. Continuously, the primary auxiliary diode Da1 is conducted.

Mode 3 [t2 – t3]: At t2, the auxiliary switch Sa is turned ON with ZVS because the body diode has already been conducted for carrying the primary inductor current iL1. After the auxiliary inductor current iLa increases to be larger than the primary inductor current iL1, the auxiliary switch current iSa becomes positive. The discharging current from the auxiliary capacitor together with the primary inductor current iL1 releases the stored energy to the output voltage Vo. During modes 2 to 3 (t = t1 – t3), the time interval can be written as (td + da)TS. The auxiliary inductor current iLa and the primary inductor current iL1 can be expressed as where IL1 is the average value of the secondary inductor current iL2, and ΔiL1 is the corresponding peak-to-peak current ripple. At t3, the local maximum value of the auxiliary inductor current iLa can be calculated as

\[ i_{La}(t) = \frac{(V_a - V_o)(t - t_1)}{L_a} \]  \hspace{1cm} (1)

\[ i_{L1}(t) = (I_{L1} + 0.5\Delta i_{L1}) + \frac{(V_1 - V_o)(t - t_1)}{L_1} \]  \hspace{1cm} (2)

where IL1 is the average value of the primary inductor current iL1, and ΔiL1 is the corresponding peak-to-peak current ripple. Note that, the time interval (t1–t2) in mode 2 is extremely short so that it could be regarded as the same time in Fig. 4. At t3, the maximum values of the auxiliary inductor current iLa can be calculated as

\[ i_{La}(t_3) = \frac{(V_a - V_o)(d_d + d_a)T_S}{L_a} \]  \hspace{1cm} (3)

According to (2), the current ripple ΔiL1 can be rewritten as

\[ \Delta i_{L1} = \frac{(V_a - V_1)(d_d + d_a)T_S}{L_1} \]  \hspace{1cm} (4)

Mode 4 [t3 – t4]: At t3, the auxiliary switch Sa is turned OFF. Because the auxiliary inductor current iLa is greater than the primary inductor current iL1, the parasitic capacitor of the auxiliary switch Sa is charged by the auxiliary inductor current iLa so that the auxiliary switch voltage vSa rises. At the same time, the energy stored in the parasitic capacitor of the switch S1 will release to the output voltage Vo via the inductor current iLa so that the switch voltage vS1 decreases. The switch current iSa falls down to zero and the switch voltage vSa rises to the auxiliary capacitor voltage Va. The body diode of the switch S1 is conducted for carrying the differential current without strain. Besides, the auxiliary inductor voltage vLa becomes positive. During modes 4 to 5 (t = t3 – t5), the time interval can be written as (dd + dcm)TS. The auxiliary inductor current iLa and the primary inductor current iL1 can be expressed as

\[ i_{La}(t) = \frac{[(V_a - V_o)(d_d + d_a)T_S - V_o(t - t_3)]}{L_a} \]  \hspace{1cm} (5)

\[ i_{L1}(t) = (I_{L1} - 0.5\Delta i_{L1}) + \frac{V_1(t - t_3)}{L_1} \]  \hspace{1cm} (6)

Mode 5 [t4 – t5]: At t4, the switch S1 is turned ON with ZVS upon the condition that the auxiliary inductor current iLa is still larger than the primary inductor current iL1. The auxiliary inductor current iLa continuously decreases with the slope −Vo/La. After the current iLa is smaller than the primary inductor current iL1, the switch current iS1 is positive. During modes 4 to 5 (t = t3 – t5), the time interval can be written as (dd + dcm)TS. The auxiliary inductor current iLa and the primary inductor current iL1 can be expressed as

\[ i_{La}(t) = \frac{(V_a - V_o)(d_d + d_a)T_S - V_o(t - t_3)}{L_a} \]  \hspace{1cm} (5)

\[ i_{L1}(t) = (I_{L1} - 0.5\Delta i_{L1}) + \frac{V_1(t - t_3)}{L_1} \]  \hspace{1cm} (6)

Mode 6 [t5 – t6]: At t5, the auxiliary inductor current iLa is equal to zero. Substituting iLa(t5) = 0 into (7), the relation between the voltages Va and Vo can be derived as
In this mode, the parasitic capacitor of the primary auxiliary diode $D_{a1}$ is charged by the output voltage $V_o$ with a small reverse-recovery current.

Mode 7 [$t_6$–$t_7$]: At $t_6$, the diode voltage $v_{D_{a1}}$ is rising to the output voltage $V_o$, the secondary auxiliary diode $D_{a2}$ is conducted for receiving the auxiliary inductor current $i_{L_a}$ to charge the auxiliary capacitor voltage $V_a$, and then the auxiliary inductor current $i_{L_a}$ returns to zero. In the single power-supply state with the primary input power, the switch $S_P$ is always turned OFF and the switch $S_2$ is triggered all the while. It means that the switch $S_2$ works as a synchronous rectifier for avoiding the current to flow through its body diode and reducing the power losses in modes 2–7 in Fig. 4.

According to the volt–second balance theory [20], the voltage–second production of the primary inductor $L_1$ in a switching period should be equal to zero. Thus, one can obtain

$$V_1(d_1 + d_d)T_S + (V_1 - V_o)(d_a + d_d)T_S = 0 \tag{8a}$$

$$V_1 = V_o(d_a + d_d). \tag{8b}$$

Assume that the dead-time duty cycle $d_d$ is much smaller than the duty cycle of the switch $d_1$; the summation of the duty cycles $d_1$ and $d_a$ approaches to 1. The relationships of (7) and (8b) can be represented as

$$V_o = \frac{(1 - d_1)V_o}{(1 + d_d - d_1)} \tag{9a}$$

$$V_1 = (1 - d_1)V_o \tag{9b}$$

$$\frac{V_o}{V_1} = \frac{1}{(1 + d_d - d_1)}. \tag{9c}$$

Because the average current of the output capacitor $C_o$ should be zero over a switching period for a constant output voltage $V_o$, the balance equation can be expressed via (3) as

$$\frac{0.5(V_o - V_o)(1 - d_1)T_S(1 - d_1 + d_{d_{em}})}{L_a} = \frac{V_o}{R_o}. \tag{10}$$

From the algebraic operation via (9) and (10), the duty cycle and the voltage gain of the converter can be derived as

$$d_{d_{em}} = 0.5(1 - d_1) \left[ \sqrt{1 + \frac{8L_o}{R_o T_S (1 - d_1)^2}} - 1 \right] \tag{11a}$$

$$V_o = \frac{2V_1}{(1 - d_1)} \left[ 1 + \sqrt{1 + \frac{8L_o}{R_o T_S (1 - d_1)^2}} \right]. \tag{11b}$$
By the similar derivation process, the voltage gain of the single power-supply state with the secondary
input power source also can be represented as

\[ V_a = \frac{V_2}{1 - d_2} \]  \hspace{1cm} (12a) 

\[ V_o = \frac{2V_2}{(1 - d_2)[1 + \sqrt{1 + \frac{8L_o}{R_oT_S(1 - d_2)^2}}]} \]  \hspace{1cm} (12b) 

where \( d_2 \) denotes the duty cycle of the switch S2.

B. Dual Power-Supply State

When the proposed converter is operated in the dual powersupply state with two input power sources, it can be taken as a superposition process of the primary and secondary input circuits. In this state, the summation of duty cycles \( d_1 \) and \( d_2 \) should be greater than 1, i.e., each of duty cycles \( d_1 \) and \( d_2 \) is securely greater than 0.5. Moreover, the symbols \( da1 \) and \( da2 \) denote the first and the second duty cycles of the switch Sa, respectively. \( \text{d} \text{dcm}1 \) and \( \text{d} \text{dcm}2 \) present the first and the second duty cycles of the freewheeling times of the auxiliary inductor. The auxiliary inductor is also designed to operate in the DCM. In order to explain the operational principle in the dual powersupply state easily, the following theoretical analysis is based on the assumption of \( iL1 > iL2 > |iL1 - iL2| \), where \( | \cdot | \) is the absolute operator. The characteristic waveforms and topological modes of the dual power-supply state are depicted in Figs. 5 and 6, respectively. Note that the time intervals in modes 2, 4, 9, and 11 are extremely short so that each interval could be regarded as the same time in Fig. 5. The operation modes in this state are discussed as follows.

Mode 1 \([t_0 \rightarrow t_1]\): At \( t_0 \), the auxiliary inductor current \( iLa \) returned to zero. The switches S1 and S2 are continuously conducted. The auxiliary switch Sa is still turned OFF. The inductors L1 and L2 are linearly charged by the input voltages \( V_1 \) and \( V_2 \), respectively.

Mode 2 \([t_1 \rightarrow t_2]\): At \( t_1 \), the switch S2 is turned OFF, the switch voltage \( vS2 \) is rising to the auxiliary capacitor voltage \( V_a \), and the auxiliary switch voltage \( vSa \) is decreasing to zero. The body diode of the auxiliary switch Sa is conducted for receiving the secondary inductor current iL2 to charge the auxiliary capacitor. Therefore, the switch current iSa is negative. Besides, the auxiliary inductor current iLa linearly increases, and the slope is dependent on the auxiliary inductor voltage \( vLa \), which is equal to \( V_a - V_o \). Continuously, the primary auxiliary diode Da1 is conducted.

\[ i_{La}(t) = \frac{(V_a - V_o)(t - t_1)}{L_a} \]  \hspace{1cm} (13) 

Mode 3 \([t_2 \rightarrow t_3]\): At \( t_2 \), the auxiliary switch Sa is turned ON with ZVS. After the auxiliary inductor current iLa increases to be larger than the secondary inductor current iL2, the auxiliary switch current iSa becomes positive. The discharging current from the auxiliary capacitor together with the secondary inductor current iL2 releases the stored energy to the output voltage \( V_o \). During modes 2 to 3 \((t = t_1 \rightarrow t_3)\), the time interval can be written as \((\text{dd} + \text{d}a2)T_S\) . The auxiliary inductor current iLa and the secondary inductor current iL2 can be expressed as

\[ i_{L2}(t) = (I_{L2} + 0.5\Delta i_{L2}) + \frac{(V_2 - V_a)(t - t_1)}{L_2} \]  \hspace{1cm} (14) 

where \( IL2 \) is the average value of the secondary inductor current iL2, and \( \Delta iL2 \) is the corresponding peak-to-peak current ripple. At \( t_3 \), the local maximum value of the auxiliary inductor current iLa can be calculated as

\[ i_{La}(t_3) = \frac{(V_a - V_o)(\text{d}a + \text{d}a2)T_S}{L_a}. \]  \hspace{1cm} (15) 

According to (14), the current ripple \( \Delta iL2 \) can be represented as

\[ \Delta i_{L2} = \frac{(V_a - V_o)(\text{d}a + \text{d}a2)T_S}{L_2}. \]  \hspace{1cm} (16) 

In addition, applying Kirchhoff’s current law, the current loop equation is given by \( iL1 = iS1 + iL2 \). The switch current iS1 can be expressed as \( iL1 - iL2 \), and it is positive so far due to the current relationship \( iL1 > iL2 \). By the topological design and switching mechanism, the conduction loss of the switch S1 sustaining all the primary inductor current iL1 can be effectively reduced, especially in the low-voltage high-current clean-energy applications.
Mode 4 \( [t_3 \rightarrow t_4] \): At \( t_3 \), the auxiliary switch \( S_a \) is turned OFF. Because the auxiliary inductor current \( i_{La} \) is greater than the secondary inductor current \( i_{L2} \), the parasitic capacitor of the auxiliary switch \( S_a \) is charged by the auxiliary inductor current \( i_{La} \), and the auxiliary switch voltage \( v_{Sa} \) rises. At the same time, the energy stored in the parasitic capacitor of the switch \( S_2 \) will release to the output voltage \( V_o \) via the inductor current \( i_{La} \), and the switch voltage \( v_{Sa} \) decreases. The switch current \( i_{S} \) falls down to zero and the switch voltage \( v_{Sa} \) rises to the auxiliary capacitor voltage \( V_a \).

The body diode of the switch \( S_2 \) is conducted for carrying the differential current without strain. Besides, the auxiliary inductor voltage \( v_{La} \) is equal to \( -V_o \), and the current \( i_{La} \) linearly decreases. The energy stored in the auxiliary inductor \( La \) starts to discharge into the output voltage \( V_o \) as freewheeling.

Mode 5 \( [t_4 \rightarrow t_5] \): At \( t_5 \), the switch \( S_2 \) is turned ON with ZVS upon the condition that the auxiliary inductor current \( i_{La} \) is still larger than the secondary inductor current \( i_{L2} \). The auxiliary inductor current \( i_{La} \) continuously decreases with the slope \( -V_o/La \). After the current \( i_{La} \) is smaller than the secondary inductor current \( i_{L2} \), the switch current \( i_{S} \) is positive. By the same way, the switch current \( i_{S} \) becomes positive as well as \( i_{S} \). During modes 4 to 5 \( (t = t_3 \rightarrow t_5) \), the time interval can be written as \((dd + ddc_m)TS \). The auxiliary inductor current \( i_{La} \) and the secondary inductor current \( i_{L2} \) can be expressed as

\[
\begin{align*}
i_{La}(t) &= \frac{(V_a - V_o)(dd + ddc_m)TS - V_o(t - t_3)}{La} \quad (17) \\
i_{L2}(t) &= (I_{L2} - 0.5\Delta I_{L2}) + \frac{V_2(t - t_3)}{L_2}. \quad (18)
\end{align*}
\]

Mode 6 \( [t_5 \rightarrow t_6] \): At \( t_5 \), the auxiliary inductor current \( i_{La} \) is equal to zero. Substituting \( i_{La}(t_5) = 0 \) into (17), the relation between the voltages \( V_a \) and \( V_o \) can be derived as

\[
(V_a - V_o)(dd + ddc_m) = V_o(dd + ddc_m). \quad (19)
\]

In this mode, the parasitic capacitor of the primary diode \( Da_1 \) is charged by the output voltage \( V_o \) with a small reverse-recovery current.

Mode 7 \( [t_6 \rightarrow t_7] \): At \( t_6 \), the diode voltage \( v_{Da1} \) is rising to the output voltage \( V_o \), the secondary auxiliary diode \( Da_2 \) is conducted for receiving the auxiliary inductor current \( i_{La} \) to charge the auxiliary capacitor.

Mode 8 \( [t_7 \rightarrow t_8] \): At \( t_7 \), the auxiliary inductor current \( i_{La} \) returns to zero. The switches \( S_1 \) and \( S_2 \) are continuously conducted. Mode 8 is similar to mode 1.

Mode 9 \( [t_8 \rightarrow t_9] \): At \( t_8 \), the switch \( S_1 \) is turned OFF, the switch voltage \( v_{S1} \) is rising to the auxiliary capacitor voltage \( V_a \), and the auxiliary switch voltage \( v_{Sa} \) is decreasing to zero. The body diode of the auxiliary switch \( S_a \) is conducted for carrying the primary inductor current \( i_{L1} \) to charge the auxiliary capacitor.

The auxiliary inductor current \( i_{La} \) linearly increases with the slope \( (V_a - V_o)/La \). Continuously, the primary auxiliary diode \( Da_1 \) is conducted.

Mode 10 \( [t_9 \rightarrow t_{10}] \): At \( t_9 \), the auxiliary switch \( S_a \) is turned ON with ZVS. After the auxiliary inductor current \( i_{La} \) becomes positive as well as \( i_{S} \), the auxiliary switch current \( i_{Sa} \) becomes positive. The discharging current from the auxiliary capacitor together with the primary inductor current \( i_{L1} \) releases the stored energy to the output voltage \( V_o \).
Mode 10 \([t_9 \rightarrow t_{10}]\): At \(t_9\), the auxiliary switch \(S_a\) is turned ON with ZVS. After the auxiliary inductor current \(i_{La}\) increases to be larger than the primary inductor current \(i_{L1}\), the auxiliary switch current \(i_{Sa}\) becomes positive. The discharging current from the auxiliary capacitor together with the primary inductor current \(i_{L1}\) releases the stored energy to the output voltage \(V_o\). During modes 9to10 \((t_{t8} \rightarrow t_{10})\), the time interval can be written as \((dd + da_1)TS\). The auxiliary inductor current \(i_{La}\) and the primary inductor current \(i_{L1}\) can be expressed as auxiliary switch \(S_a\) is charged by the auxiliary inductor current \(i_{La}\). At the same time, the energy stored in the parasitic capacitor of the switch \(S_1\) will release to the output voltage \(V_o\) via the inductor current \(i_{La}\). The switch current \(i_{Sa}\) falls down to zero and the switch voltage \(v_{Sa}\) rises to the auxiliary capacitor voltage \(V_a\). Similar to mode 4, both the switches' currents \(i_{S1}\) and \(i_{S2}\) are negative.
The energy stored in the auxiliary inductor \( L_a \) starts to discharge into the output voltage \( V_o \) as freewheeling.

Mode 12 \([t11\sim t12]\): At \( t11 \), the switch \( S1 \) is turned ON with ZVS. The auxiliary inductor current \( i_{La} \) initially decreases with the slope \(-V_o/L_a\). After the current \( i_{La} \) is smaller than the primary inductor current \( i_{L1} \), the switch current \( i_{S1} \) is positive. By the same way, the switch current \( i_{S2} \) becomes positive as well as \( i_{S1} \). During modes \( 11 \) to \( 12 \) (\( t = t11 \sim t12 \)), the time interval can be written as \((dd + d_{dc1}t)/TS\). The auxiliary inductor current \( i_{La} \) and the primary inductor current \( i_{L1} \) can be expressed as:

\[
i_{La}(t) = \frac{[V_a - V_o](dd + d_{a1})TS - V_o(t - t_{10})]}{L_a}
\]

\[
i_{L1}(t) = \left( I_{L1} - 0.5\Delta i_{L1} \right) + \frac{V_a(t - t_{10})}{L_1}
\]

Mode 13 \([t12\sim t13]\): At \( t12 \), the auxiliary inductor current \( i_{La} \) is equal to zero. Substituting \( i_{La}(t12) = 0\) into (24), the relation between the voltages \( V_a \) and \( V_o \) can be derived as:

\[
V_a - V_o(dd + d_{a1}) = V_o(dd + d_{dc1}).
\]

Mode 13 is similar to mode 6 as well as the reverse-recovery time of the primary auxiliary diode Da1. Mode 14 \([t13\sim t14]\): At \( t13 \), the diode voltage \( V_{Da1} \) is rising to the output voltage \( V_o \) and the secondary auxiliary diode Da2 is conducted for receiving the auxiliary inductor current \( i_{La} \) to charge the auxiliary capacitor. According to the volt–second balance theory [20], the voltage second productions of the inductors \( L1 \) and \( L2 \) in a switching period should be equal to zero. Thus, one can obtain Assume that the dead-time duty cycle \( dd \) is much smaller than the duty cycles of the switches \( d1 \) and \( d2 \), the relationships of the voltages in (19), (26), (27c), and (27d) can be rewritten as:

\[
V_o = \frac{(1 - d1)V_a}{(1 + d_{dc1} - d1)} = \frac{(1 - d2)V_a}{(1 + d_{dc2} - d2)},
\]

\[
V_a = \frac{V_1}{(1 - d1)} = \frac{V_2}{(1 - d2)}.
\]

Equations (30c) and (31) state that the proposed converter can simultaneously boost both input power sources with different voltage levels to a stable output voltage via controlling the driving signals of the switches \( T1, T2, \) and \( Ta \). Moreover, there exists only one pair of the duty cycles \( d1 \) and \( d2 \) according to specific input voltages. Note that the driving signal \( Ta \) is composed of \( T1 \) and \( T2 \) as shown in Fig. 5. First, one should make up the inverse signals of \( T1 \) and \( T2 \) as \( T1 \) and \( T2 \). Then, the inverse signals \( T1 \) and \( T2 \) are processed through delay time functions to synthesize the signals \( T_{11} \) and \( T_{22} \). In the driving circuit, the control signals \( T_{1} \) and \( T_{2} \) are passed through logic OR gate IC to compose the driving signal \( Ta \) for the auxiliary switch. In this study, a high-efficiency ZVS dual-input converter is investigated. The proposed converter utilizes the primary and secondary input circuits to be connected in series and operates in continuous conduction mode (CCM). The phenomenon of a high reverse-recovery current in a traditional step-up converter will be greatly alleviated via the utilization of an auxiliary inductor in series connected with a diode when the diode current falls to zero. If the primary and secondary input circuits are changed to connect in parallel, the primary inductor \( L1 \) and the secondary inductor \( L2 \) can be operated in DCM. In this case, the control signals for the primary and secondary input circuits are different from the ones for these two input circuits connected in series. The control signals for the primary and secondary input circuits connected in parallel can be widely designed without regard to the series-inductor problem. Moreover, it would reduce the inductor volume and save two level shifter circuits for the floating switches. However, the primary inductor \( L1 \) and the secondary inductor \( L2 \) operated in DCM would cause the inductor currents \( iL1 \) and \( iL2 \) with higher peak values, so that the lifetime of the input power source (e.g., battery module or FC) will be degenerated. Besides, the DCM operation is not suitable for a high-power application.

**IV. CONCLUSION**

The effectiveness of this converter is also verified by the experimental results. In the single power-supply state, the property of ZVS turn ON of all switches guarantees that switching losses can be reduced. In the dual power-supply state, the conduction loss can be effectively reduced by topological design of series connection of two input circuits. Besides, the reverse-recovery currents of the diodes are slight as well as the switching losses of the switches are effectively
reduced. The maximum efficiency of the proposed converter operated in both operational states is higher than 95%. This new converter topology provides designers with an alternative choice to simultaneously convert hybrid power sources. In addition, the proposed high-efficiency dual-input converter also can work well in high-power level applications because the switching losses can be greatly reduced due to the ZVS property. In general, the ground leakage current would be harmful to high-power nonisolated PV applications due to the presence of a parasitic capacitance between the PV cells and the metal frame of the PV panel, usually connected to earth. A two-stage PV ac-module application including a nonisolated high step-up dc/dc converter and a newly designed H6-type dc/ac inverter to feature high efficiency over a wide load range, low ground leakage current, no need for split capacitors, and low-output ac-current distortion. If the proposed ZVS dual-input converter in this study is used for nonisolated PV applications, the ground leakage current issue due to the high-frequency voltage swing between the two negative terminals of the input sources also may cause safety and electromagnetic interference (EMI) problems because the input power sources do not share the same ground. These problems could be solved by the adoption of an EMI filter.

IV REFERENCES


