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Research Article

High speed fir filters using add and shift method based on FPGA

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ABSTRACT

In this paper, a method for implementing high speed Finite Impulse Response (FIR) filters using just registered adders and hardwired shifts is presented. A modified common subexpression elimination algorithm is extensively used to reduce the number of adders. The target is on optimizations to Xilinx Virtex II devices where the implementations are compared with those produced by Xilinx CoregenTM using Distributed Arithmetic. It is observed that up to 50% reduction in the number of slices and up to 75% reduction in the number of LUTs for fully parallel implementations and also observed up to 50% reduction in the total dynamic power consumption of the filters. The designs implemented in this method perform significantly faster than the MAC filters, which use embedded multipliers.

Keywords: Combinational Logic Blocks, Finite Impulse Response Filter, Multiply and Accumulate, Look up Table.

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