



Research Article



Low Power Multiplier to Reduce Switching Activities Using Bypassing Technique

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ABSTRACT

Multipliers and adders are the basic circuits required for implementing any Arithmetic and logic functions in VLSI. Many of the real-time applications like the arithmetic operations in Microprocessor, the filter designing in Signal processing require the multipliers. As the multipliers play a major role in the VLSI designing the power consumption related to them is a parameter to be thought of. To achieve such power reduction, modifications are made to conventional multiplier architecture and low power multiplier architecture is proposed using a technique called bypassing in this work. This proposed architecture removes the unnecessary switching activities responsible for power consumption and also eliminates unnecessary iteration done in the conventional multiplier whenever a zero is encountered in the multiplier.

Keywords: low power, multiplier, shift-and-add, ring counter, feeder.

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