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Energy Efficient Reversible logic Design for Code Converters

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This paper proposes a new 3×3 reversible logic gates for application in optimized code converters. An optimum reversible logic design for different code converters such as BCD to Excess-3, Excess-3 to BCD, Binary to Gray and Gray to Binary is achieved by using the proposed reversible logic gates. It was shown that the proposed design leads to the reduction of power consumption compared with conventional logic circuits. This optimization is achieved by minimizing number of logic gates, garbage values and input constants.

Keywords: code converters; garbage values; reversible logic gates;

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ELECTRONICS RESEARCH ARTICLE

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ABSTRACT

This paper proposes a new 3×3 reversible logic gates for application in optimized code converters. An optimum reversible logic design for different code converters such as BCD to Excess-3, Excess-3 to BCD, Binary to Gray and Gray to Binary is achieved by using the proposed reversible logic gates. It was shown that the proposed design leads to the reduction of power consumption compared with conventional logic circuits. This optimization is achieved by minimizing number of logic gates, garbage values and input constants.

Keywords: code converters; garbage values; reversible logic gates;

1. INTRODUCTION

Power consumption plays a significant role in the present day VLSI technology. So energy efficiency has become main concern in the portable equipments to get better performance with less power dissipation [1]. Reversible logic has received significant attention in recent years to achieve optimum power consumption [2]. Reversible computing is a model of computing where the computational process to some extent is reversible, i.e., time-invertible. In a computational model that uses transitions from one state of the abstract machine to another, a necessary condition for reversibility is that the relation of the mapping from states to their successors must be one-to-one. Reversible computing is generally considered an unconventional form of computing. Broadly, there are two different levels of reversible computing: Logically reversible computing means computing in such a way that it always remains possible to efficiently reconstruct the previous state of the computation from the current state. Doing this enables thermodynamically reversible computing which generates no (or very little) new physical entropy, and is thus energy efficient [2].

Recently, in [3-4], reversible logic gates and reversible circuits for realizing different code converters like BCD to Excess-3, Excess-3 to BCD, Binary to Gray and Gray to Binary was proposed and it was shown that the proposed design leads to the reduction of power consumption compared with conventional logic circuits, the design proposed was implemented with Feynman gate (FG) and URG gates described in [4].

In this paper, new reversible logic gates for optimization of power consumption are proposed and designed. This optimization of power is obtained by minimizing number of garbage values, input constants and finally number of logic gates. Further, reversible code converters for binary to gray, gray to binary, BCD to excess-3 and excess-3 to BCD with proposed reversible logic gates are implemented and compared with earlier designs [4].

2. Proposed Reversible Logic Gates

Basic concepts of reversible logic gates and various reversible logic gates proposed are discussed in this section. A $n\times n$ reversible gate can be represented as [4]

$$IV = (A, B, C, \ldots)$$
$$OV = (P, Q, R, \ldots) \quad (1)$$

Where IV and OV are input and output vectors. Truth tables of proposed gates are listed in Table I to Table V.

I. TRUTH TABLE OF NG1 GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

II. TRUTH TABLE OF NG2 GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	1	1	1

III. TRUTH TABLE OF NG3 GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	0	0

IV. TRUTH TABLE OF NG4 GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

V. TRUTH TABLE OF NG5 GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

Existing reversible gates and proposed reversible logic gates are listed in Table VII and VIII respectively (shown at the end of the paper).

Few frequently used codes in digital systems are Binary, Binary Coded Decimal, Excess-3, Gray, ASCII etc. A code converter can be implemented by using a circuitry of AND, OR and NOT gates. In the following section few code converters are designed and implemented using the reversible logic gates described in Table I and II.

3. Reversible Binary to Gray and Gray to Binary Converter

Fig. 1 and 2 shows the circuit diagrams of reverse Binary to Gray and Gray to Binary code converter respectively. Here 'G' represents the garbage value. In the designing of Binary to Gray Code Converter one garbage value is generated, no. of input constants is zero and no. of reversible logic gates required is two. Thus with the proposed reversible gates a Gray to Binary Code Converter can be developed in such a way that the no. of input constants and generated garbage values are zero and no. of gates used is two.

Further, the no. of input constants, garbage values generated and no. of reversible logic gates are used to implement these code converters are less when compared to the conventional reversible logic gates [4-5].

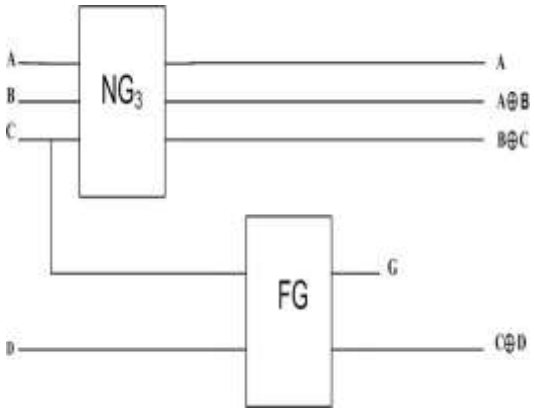


Figure1: Circuit diagram of Reversible Binary to Gray Code Converter.

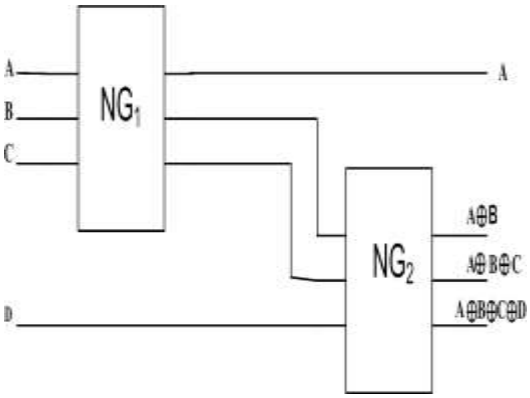


Figure2: Circuit diagram of Reversible Gray to Binary Code Converter.

4. Reversible BCD to Excess-3 and Excess-3 to BCD Converter

Fig. 2 (a) and (b) shows the circuit diagrams of Reverse BCD to Excess-3 and Excess-3 to BCD converter respectively. In designing of BCD to Excess-3 code converter ten garbage values are generated, no. of input constants is three and no. of reversible logic gates required is six. Thus with the proposed reversible gates a Excess-3 to BCD Code Converter is designed in such a way that the no. of input constants is three, generated garbage values are seven and no. of gates used is five.

Further, the no. of input constants, garbage values generated and no. of reversible logic gates are used to implement these code converters are less when compared to the previous designs [4-5].

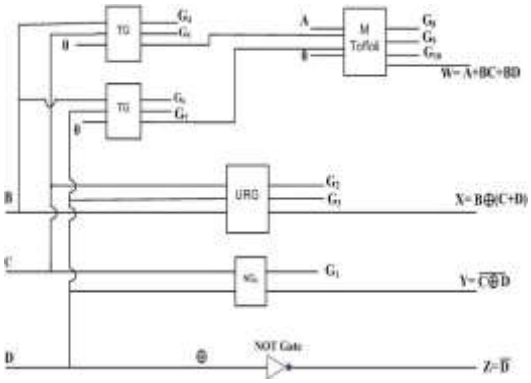


Figure3: Circuit diagram of Reversible BCD to Excess-3 Code Converter.

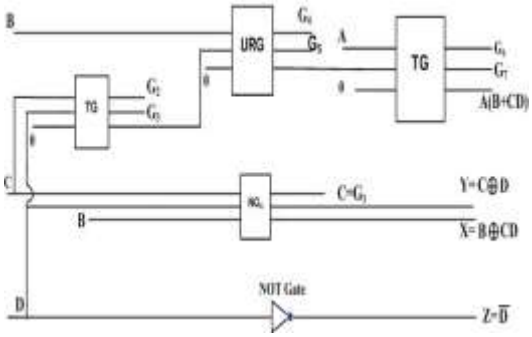


Figure4: Circuit diagram of Reversible Excess-3 to BCD Code Converter.

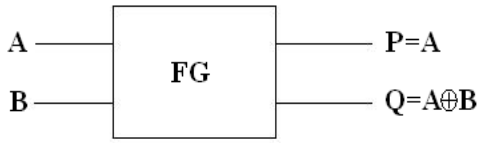
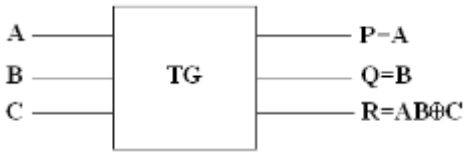
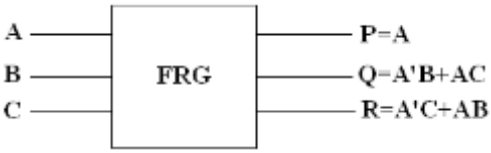
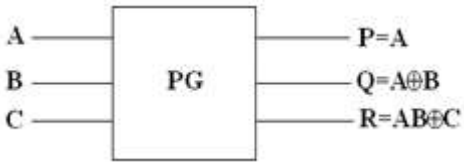
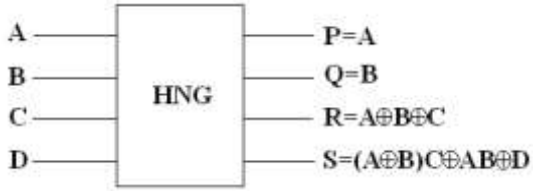
5. Performance Analysis

The performance of the design is based on the number of gates, number of garbage (unused terminals) values and number of constants. Table IX provides a summary of the proposed design. It is observed from Table IX that the proposed design achieves optimization by minimizing the number of gates, garbage values and input constants when compared to earlier designs described in [4-5].

VI. PROPOSED DESIGN

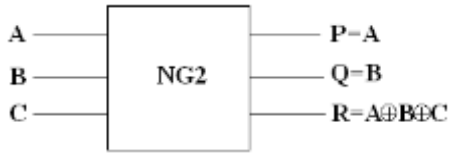
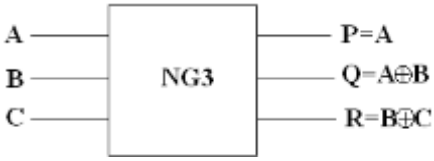
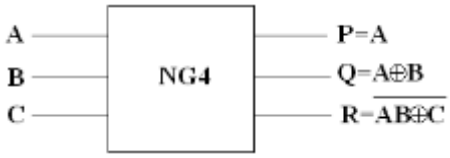
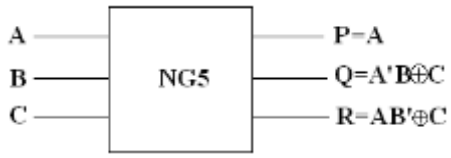
Reversible Code Converters	No. of gates	No. of garbage values	No. of input constants
Binary to Gray	2	1	0
Gray to Binary	2	0	0
BCD to Excess-3	6	10	3
Excess-3 to BCD	5	7	3

VII. EXISTING REVERSIBLE LOGIC GATES

Gate	Diagrammatic representation	Inputs	Outputs
Feyman Gate		A, B	P, Q $P = A$ $Q = A \oplus B$
Toffoli Gate		A, B, C	P, Q, R $P = A$ $Q = B$ $R = AB \oplus C$
Fredkin Gate		A, B, C	P, Q, R $P = A$ $Q = A'B \oplus AC$ $R = A'C \oplus AB$
Peres Gate		A, B, C	P, Q, R $P = A$ $Q = A \oplus B$ $R = AB \oplus C$
URG Gate		A, B, C	P, Q, R $P = C \oplus AB$ $Q = B$ $R = C \oplus (A + B)$
HNG Gate		A, B, C, D	P, Q, R, S $P = A$ $Q = B$ $R = A \oplus B \oplus C$ $S = (A \oplus B)C \oplus AB \oplus D$

VIII. PROPOSED REVERSIBLE LOGIC GATES

Gate	Diagrammatic representation	Inputs	Outputs
NG1		A, B, C	P, Q, R $P = A$ $Q = A \oplus B$ $R = A \oplus B \oplus C$

Gate	Diagrammatic representation	Inputs	Outputs
NG2		A, B, C	P, Q, R $P = A$ $Q = B$ $R = A \oplus B \oplus C$
NG3		A, B, C	P, Q, R $P = A$ $Q = A \oplus B$ $R = B \oplus C$
NG4		A, B, C	P, Q, R $P = A$ $Q = A \oplus B$ $R = \overline{AB \oplus C}$
NG5		A, B, C	P, Q, R $P = A$ $Q = A'B \oplus C$ $R = AB' \oplus C$

6. CONCLUDING REMARKS

New reversible logic gates were proposed in this paper and reversible circuits for realizing different code converters like Binary to Gray, Gray to Binary, BCD to Excess-3 and Excess-3 to BCD were analyzed. The proposed design is optimum in terms of the reduction of power consumption compared with previous logic circuits, i.e., the proposed design increases the energy efficiency by minimizing no. of gates, garbage values and input constants.

REFERENCES

1. A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low power CMOS digital design," IEEE J. Solid-State Circ., vol. 27, no. 4, pp.473-484, Apr. 1992.
2. http://www.cise.utl.edu/research/revcmp/
3. Raghava Garipelly, P.Madhu Kiran and A.Santhosh Kumar, "A Review on Reversible Logic Gates and their Implementation," International Journal of Emerging Technology and Advanced Engineering, Vol. 3, Issue 3, March 2013.
4. M. Saravanan and K. Suresh Manik, "Energy Efficient Code Converters using Reversible Logic Gates," Proc. of 2013 International Conference on Green High Performance Computing, March 14-15, 2013, India.
5. B. Dilli Kumar and M. Bharathi, "Design of Energy Efficient Binary to Excess-3 Converter Using Adiabatic Techniques," International Journal Computer Applications in Engineering Sciences, pp. 14-19, Vol. III, Issue I, March 2013.
6. Designing low power multipliers" IEEE Trans. Very Large Scale Integer (VLSI)Syst., Vol.11, No-3, pp418-433, June 2003
7. Zamin Ali Khana ,S. M. Aqil Burneyb, , Jawed Naseemc, Kashif Rizwand, "Optimization of Power Consumption in VLSI Circuit", IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 2, March 2011
8. K.H.Chen and Y.S.Chu , "A low power multiplier with spurious power suppression technique" ,IEEE Trans. Very Large Scale Integr .(VLSI)Syst. , Vol.15 , no-7,pp846-850, July 2007.
9. V. P. Nelson, H. T. Nagle, B. D. Carroll, and J. I. David,"Digital Logic Circuit Analysis & Design." Englewood Cliffs, NJ: Prentice-Hall, 1996.