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Research Article

Design and implementation of online BIST for different word sizes of memories

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ABSTRACT

Transparent BIST schemes for RAM modules assure the preservation of the memory contents during periodic testing Symmetric Transparent Built-in Self-Test (BIST) schemes skip the signature prediction phase required in traditional transparent BIST. Achieving considerable reduction in test time. Previous works or symmetric transparent BIST schemes require that a separate BIST module is utilized for each RAM under test. This approach, giver the large number of memories available in current chips, increase the hardware overhead of the BIST circuitry. In this work we propose a Symmetric transparent BIST scheme that can be utilized to test Rams. For 5 different word widths hence, more than one RAMs can be tested in a roving manner. The hardware overhead of the proposed scheme is considerably smaller compared to the utilization of previously proposed symmetric transparent schemes.

Keywords: Built-In Self-Test (BIST), Built-In Address-Analysis (BIAA), SRAM, BISR

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