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Research Article

CLAA, CSLA and PPA based Shift and Add Multiplier for General Purpose Processor

A. Sowjanya [1] and R. Mahalaxmi [2]

Corresponding Author:
sowji.sowjanya045@gmail.com

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ABSTRACT

This project deals with the comparison of the VLSI design of the carry look-ahead adder (CLAA) based 32-bit unsigned integer multiplier and the VLSI design of the carry select adder (CSLA) based 32-bit unsigned integer multiplier. Both the VLSI design of multiplier multiplies two 32-bit unsigned integer values and gives a product term of 64-bit values. The CLAA based multiplier and CSLA based multiplier uses nearly the same delay time for multiplication operation. But the area needed for CSLA multiplier is less by the CLLA based multiplier to complete the multiplication operation.PPA is used to increase the speed then CSLA and CLAA.

Keywords: CLAA, CSLA, PPA, Delay, Area, Array Multiplier, VHDL Modeling & Simulation.

[1] M.Tech (Pursuing) and [2] Assistant Professor
[1 2] Department of ECE, Malla Reddy engineering college for Women,
Affiliated to Jawarlal Nehru Technological University, Dhulapally, Secunderabad - 506 014.

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