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Research Article

# Design and Implementation of Carry Select Adder without using Multiplexer

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**ABSTRACT**

Design of high performance digital adder with reduced area and low power consumption is an important requirement in advanced digital processors for faster computation. In digital adder circuits, the speed of addition is limited by the time required for a carry to propagate through the adder. Many different approaches had already been suggested to improve the performance of the adder. Carry Select Adder is one among them and is used to solve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the final sum. The speed of operation of such an adder is limited by carry propagation from input to output. Our work is based on designing an optimized adder for advanced processors. It discuss about the implementation of Carry Select Adder without using Multiplexer for final selection. Parallel adder configuration is also used to reduce the delay between stages. Removing the MUX stage will reduce the area as well as propagation delay to give much higher performance for the adder. The Kogge Stone parallel approach will generate fast carry for intermediate stages.

**Keywords:** CSA, MUX.

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