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Op-Amps for Pipeline ADCs

Dr. P. Prasad Rao

Corresponding Author:
prasadrao_hod@yahoo.co.in

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ABSTRACT

All electrical signals in nature are analog and since most of the signal processing is done in the digital domain, Analog to Digital (ADC) and Digital to Analog (DAC) converters have become a necessity. Flash ADC makes all bit decisions in a single go while Successive approximation ADC makes single bit decision at a time. Flash ADCs are faster but area increases exponentially with bit length while successive approximation ADC is slow and occupies less area. Between these two extremes, many other architectures exist, deciding a fixed number of bits at a time such as pipeline and multistep ADCs. They balance circuit complexity and speed. For medium speed and with high resolution pipelined ADCs are promising. This paper is devoted to study the op-amp requirements for pipelined ADCs and the comparison of different op-amp architectures.

Keywords: Pipelined ADCs, Open loop gain, Unity gain frequency, folded cascode op-amp, Gain boosting technique.

Professor, Department of Electronics & Communication Engineering
Vaagdevi College Engineering (Autonomous), Affiliated to JNTUH, Warangal - 506 005.

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ELECTRONICS RESEARCH ARTICLE

Op-Amps for Pipeline ADCs

Dr. P. Prasad Rao
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Vaagdevi College Engineering (Autonomous), Affiliated to JNTUH, Warangal - 506 005.
prasadrao_hod@yahoo.co.in

ABSTRACT

All electrical signals in nature are analog and since most of the signal processing is done in the digital domain, Analog to Digital (ADC) and Digital to Analog (DAC) converters have become a necessity. Flash ADC makes all bit decisions in a single go while Successive approximation ADC makes single bit decision at a time. Flash ADCs are faster but area increases exponentially with bit length while successive approximation ADC is slow and occupies less area. Between these two extremes, many other architectures exist, deciding a fixed number of bits at a time such as pipeline and multistep ADCs. They balance circuit complexity and speed. For medium speed and with high resolution pipelined ADCs are promising. This paper is devoted to study the op-amp requirements for pipelined ADCs and the comparison of different op-amp architectures.

Keywords: Pipelined ADCs, Open loop gain, Unity gain frequency, Folded cascode op-amp, Gain boosting technique.

1. INTRODUCTION

The basic building blocks required to implement a pipeline ADC includes analog blocks like Operational amplifier, Comparator and S/H amplifier. The digital logic requirements are in Digital error correction, encoders in sub-converters, shift registers and clock generation. This paper is devoted to study the op-amp requirements for pipelined ADCs and the comparison of different op-amp architectures.

2. REQUIREMENTS OF OP-AMPS IN DATA CONVERTERS

The magnitude and phase response curves of a typical op-amp are shown in Fig.1. The gain, bandwidth requirements of an op-amp must be carefully selected if it is to be used in an N-bit A/D converter. The op-amp is assumed to have 90^0 phase margin over full load conditions by compensating it with a load capacitance C_L. If phase margin is 90^0 then we get a response similar to an RC circuit, and hence avoid overshoot and ringing. This reduces the settling time of op-amp.

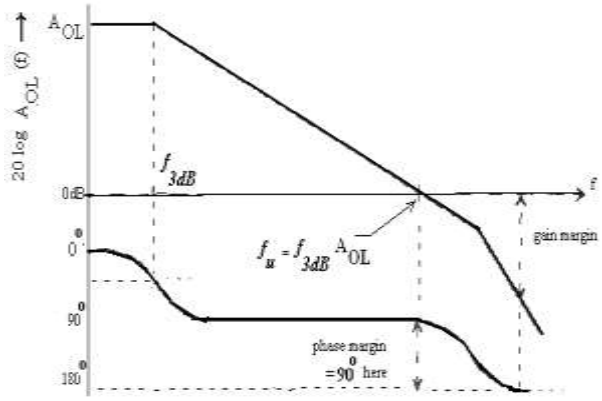

Fig.1 Magnitude and Phase response of an op-amp

2.1. Gain requirements

The op-amp in data converter must amplify the signals to ± ½ LSB of its ideal value. If the open loop gain of the amplifier of Fig. 2 is A_{OL}, then, its closed loop gain can be expressed as

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} \qquad \text{----- Eq. (1)}$$

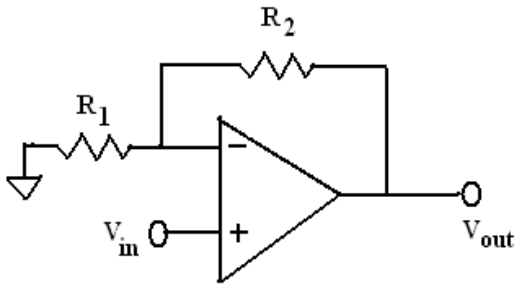

Fig. 2 Non-inverting amplifier using op-amp

and the feedback factor is

$$\beta = \frac{R_1}{R_1 + R_2} \quad \text{----- Eq. (2)}$$

Or if capacitors C_i and C_f are used then

$$\beta = \frac{C_f}{Ci + C_f} \quad \text{----- Eq. (3)}$$

And the closed loop gain A_{CL} is

$$|A_{CL}| = \frac{C_i}{C_f} \quad \text{----- Eq. (4)}$$

If the maximum deviation in gain is ΔA, then using equation ( )

$$|A_{CL}| = \frac{C_i}{C_f} - \Delta A = \frac{A_{OL}}{1 + A_{OL}\dfrac{C_f}{C_t + C_f}} \quad \text{----- Eq. (5)}$$

In data converters, the maximum variation should be within ½ LSB of the ideal value. Therefore

$$\Delta A = \frac{C_i}{C_f}\frac{\frac{1}{2}LSB}{FullScaleoutput} = \frac{C_i}{C_f}\frac{\frac{1}{2}\frac{V_{ref}}{2^N}}{V_{ref}} = \frac{C_i}{C_f}\frac{1}{2^{N+1}} \quad \text{--- Eq. (6)}$$

The minimum DC open loop gain required is

$$|A_{OL}| \geq \frac{1}{\beta} 2^{N+1} \quad \text{----- Eq. (7)}$$

If $C_i = C_f$ then $\beta = ½$ and

$$|A_{OL}| \geq \frac{1}{\beta} 2^{N+2} \quad \text{----- Eq. (8)}$$

i.e., for a 10-bit ADC, the op-amp must have a gain greater than 4K.

2.2 Unity gain frequency requirements

The architecture used decides the speed of an op-amp [1]. The op-amp must settle to with ± ½ LSB in the least time possible. The output of an op-amp can be expressed as

$V_{out} = V_{outfinal}(1\text{-}e\text{-}t/\tau)$ ----- Eq. (9)

For output equal to ½ LSB,

$$\frac{1}{2^{N+1}} = 1 - \frac{V_{out}}{V_{outfinal}} = e^{-tsettling/\tau} \quad \text{----- Eq. (10)}$$

Where $t_{settling} = \tau \ln 2^{N+1}$ and $f_{clk} = 1/tsettling$

The time constant of the circuit is

$$\tau = \frac{1}{2\Pi\beta f_u} \quad \text{----- Eq. (11)}$$

The minimum unity gain frequency of op-amp is then given by

$$f_u \geq \frac{f_{clk} \ln 2^{N+1}}{\beta} \quad \text{----- Eq. (12)}$$

If $\beta = ½$ then

$f_u \geq 0.22\,(N+1)\,f_{clk}$ ----- Eq. (13)

Therefore a 10bit, 50Ms/sec ADC, the op-amp must have a minimum unity gain frequency of 120MHz.

3. SINGLE STAGE OP-AMPS

There are several architectures available in single stage Op-Amps viz. the simple op-amp, cascode op-amp, folded cascode op-amp and triple cascode op-amp. They can be single ended or differential.

3.1.1 Simple op-amp

Fig. 3 (a) shows a simple single ended CMOS op-amp while Fig. 3 (b) shows differential op-amp.

The low frequency small signal gain of both these circuits is

$$A = g_mN (r_oN \| r_oP) \quad \text{----- Eq. (14)}$$

Where r_oN = output resistance of NMOS

r_oP = output resistance of PMOS

g_mN = Transconductance of NMOS.

The gain achievable is about 20 and the bandwidth is determined by the load capacitance C_L.

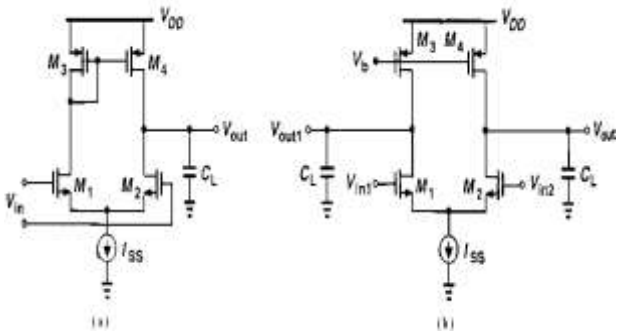

Fig.3. Simple op-amp topologies

3.1.2 Cascode op-amp

To achieve high gain, cascode topologies may be used. Fig.4 (a) shows the single ended and Fig.4 (b) shows the differential cascode op-amps or telescopic cascode op-amps. Such circuits will have a gain A, given by

$$A = g_mN [(g_mN\, r_oN^2 \| g_mP\, r_oP^2)] \quad \text{----- Eq. (15)}$$

Here, the gain is seen to be much higher than that of simple op-amp of Fig. 3. However, additional poles result in the transfer function which affects the phase margin and f_u. Also the output swing is reduced and is given by

$$V_{out}=2[V_{DD}-(V_{D1}+V_{D3}+V_{CSS}+V_{D5}+V_{D7})] - \quad \text{----Eq. (16)}$$

where V_{Di} denotes the effective gate voltage or the overdrive voltage of MOSFETs and V_{CSS} denotes the drop across the current source.

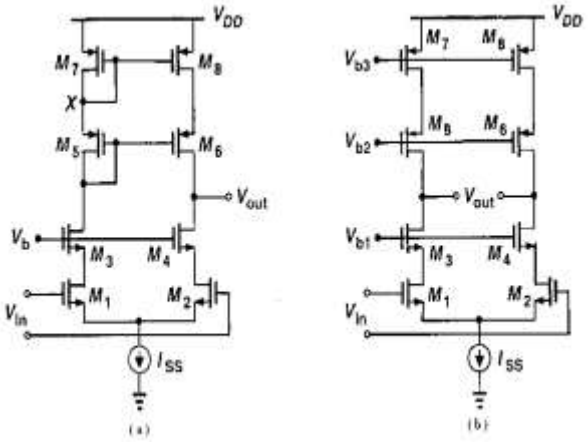

Fig. 4 Cascode op-amp architectures

In switched capacitor circuits, we need to short input and output of op-amps for some duration. But the severe drawback of telescopic cascode is that the output cannot be shorted back to input to realize unity gain buffers.

3.1.3 Folded cascode op-amp

A folded cascode op-amp can be used to overcome the drawbacks of telescopic cascode op-amps [2]-[4].

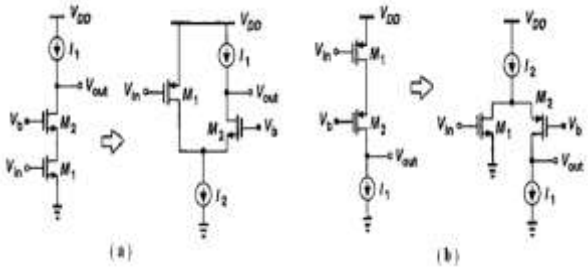

Fig. 5 Cascode op-amps

In Fig. 5(a), the NMOS cascode amplifier is converted to a folded cascode amplifier, by replacing the input NMOS by PMOS. Also in Fig. 5(b), a PMOS cascode amplifier is converted to a folded cascode amplifier by replacing the input PMOS by NMOS. In all the above circuits, the current generated by M1 flows through M2 and hence through the load to produce an output voltage.

$$V_0 = g_m\, r_{out}\, V_{in} \quad \text{----- Eq. (17)}$$

This idea can be applied to differential pairs also and hence the differential op-amps as shown in Fig. 6. A folded cascode op-amp with input NMOS driving PMOS cascode transistor provides a higher gain than a PMOS driving NMOS. This is because the mobility of charges in NMOS devices is greater. The voltage swing of folded cascode is seen to be higher compared to that of telescopic cascode structure by the threshold voltage V_t, but, at the cost of higher power dissipation, lower voltage gain and lower f_u.

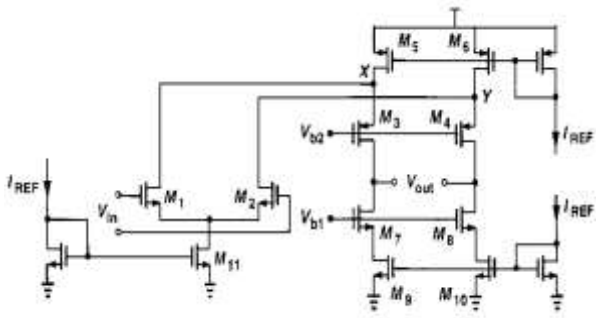

Fig.6 Differential folded cascode op-amp

3.1.4 Tripe cascode op-amp

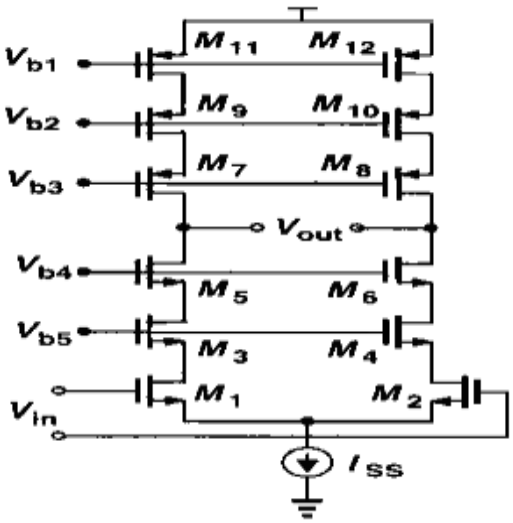

Fig. 7 Triple Cascode op-amp

To achieve still higher gains, we can cascode more number of devices as shown in Fig.7. A triple cascode typically provides a gain by $(g_m r_o)^3$ /2 but, it further reduces the output swing as six effective gate voltages must be subtracted from VDD. This op-amp cannot be operated at low voltages.

3.2 TWO STAGE OP-AMP

This op-amp uses two stages and hence provides a larger gain. Here the first stage provides a high gain and the second stage is for providing large output swing. The individual stages can use any of the single stage op-amps discussed in previous sections. The two stage differential op-amp is shown in Fig. 8.

The gain of first stage is

$A_1 = g_{m1} (r_{o1} \| r_{o3}) = g_{m2} (r_{o2} \| r_{o4})$ ----- Eq. (18)

and the gain of second stage is

$A_2 = g_{m6} (r_{o6} \| r_{o7}) = g_{m5} (r_{o5} \| r_{o7})$ ----- Eq. (19)

To obtain still higher gains, the first stage can use cascoding of devices. In two stage amplifiers, each stage introduces at least one pole in the transfer function making it more unstable. The unity gain frequency also reduces. Hence a third stage is almost never used.

3.3 GAIN BOOSTING IN OP-AMPS

Single stage op-amps have the drawback of less gain while the two stage op-amp provides more gain but at reduced speeds. This made the designers to think about new approaches. In single stage op-amps, output resistance is increased to get higher voltage gain [5] [6]. The idea of using gain boosting technique is only to increase the output resistance further.

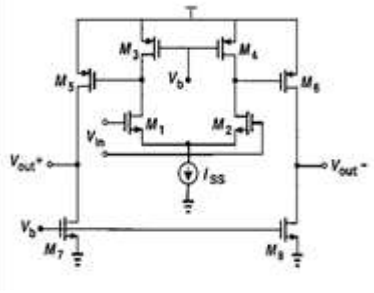

Fig.8 Simple Two stage op-amp

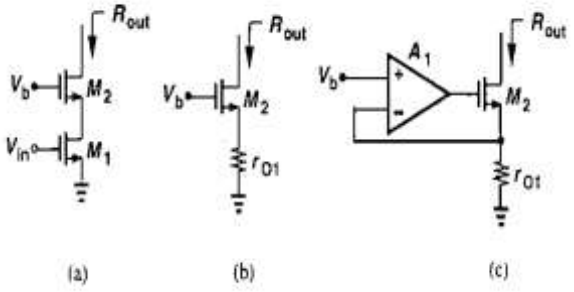

Fig.9 Gain boosting technique

Simple cascode circuit is shown in Fig. 9 (a). The output impedance of this circuit is

$$R_{out} = g_{m2} r_{01} r_{02} \quad \text{----- Eq. (20)}$$

From Fig.9 (b), it is clear that the small signal voltage produced across r_{01} is proportional to output current. If this voltage is subtracted from V_b, then the output impedance will increase. The Rout value now modifies to

$$R_{out} \approx A_1 g_{m2} r_{01} r_{02} \quad \text{----- Eq. (21)}$$

Therefore, R_{out} is 'boosted' by a good amount without cascoding more devices on top of M2.

3.4 COMPARISON OF OP-AMP TOPOLOGIES

The comparison of telescopic cascode, folded cascode, two stage op-amps and the gain boosted op-amp is shown in Table 1.

Table.1 Comparison of Various Op-Amps

Op-amp type	Gain	Output swing	Speed	Noise	Power Dissipation
Telescopic cascode	Medium	Low	Highest	Low	Low
Folded cascode	Medium	Medium	High	Medium	Medium
Two stage	High	Highest	Low	Low	Medium
Gain Boosted	High	Medium	Medium	Medium	High

From Table 1 it is clear that for low voltage and high speed applications, a folded cascode op-amp is a preferred choice.

4. IMPLEMENTING THE OP-AMP

Operational amplifier is the heart of any analog design. It is better to have op-amps with large open loop gain and unity gain frequencies for fast and accurate settling. Single ended and differential folded cascode op-amps are designed and implemented.

4.1.1 Single ended folded cascode op-amp

The modern CMOS op-amps drive capacitive loads. If load is capacitive, it is not necessary to use an output buffer to provide a low impedance node at the output. Hence, it is possible to design high speed and large output swing op-amps. This is possible by a single high impedance node at the output which drives C_L. The compensation in folded cascode op-amps is provided by C_L itself and it is dominant pole compensation. The stability of op-amp improves with an increase in C_L. However, this reduces the unity gain frequency and the speed of op-amp.

The folded cascode op-amp with single ended output is shown in Fig.10. The input is given to NMOS devices M1 and M2 which in turn drives cascoded PMOS devices M3 and M4 and hence the name folded cascode op-amp. This op-amp will have good PSRR since it is compensated with a load capacitance C_L.

If the differential pair M1, M2 is removed, then equal currents flow in M3, M4 and M10 to M15. If M1 M2 is added, then it shares the current coming from M10 M11 and hence, the current through M3 M4 and M12 to M15 reduces proportionally. MOSFETs M7,M8 and M9 provides the DC bias conditions in the network.

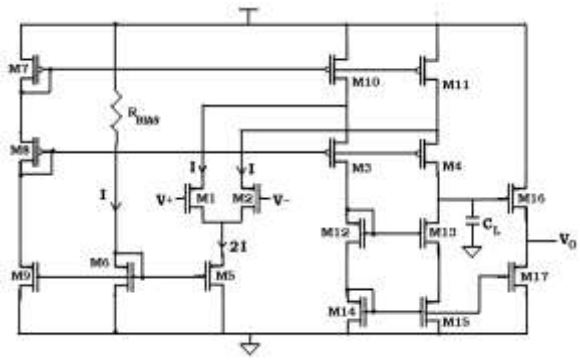

Fig. 10 Single ended Folded Cascode Op-Amp

When Vi is applied across V+ and V-, then current flows in the differential amplifier circuit M1 M2 given by

$$I_1 = I_2 = I = g_m V_i \quad \text{-----Eq. (22)}$$

The AC gain of the differential input stage is mirrored into the cascode MOSFETs, M3 and M4 and hence into the MOSFETs M12 to M15. The output voltage of the op-amp will be

$$V_0 = g_m V_i R_0 \quad \text{-----Eq. (23)}$$

Where R_0 = (Resistance looking into the drain of M13) ‖ (Resistance looking into drain of M4)

$$= [r_{013}(1 + gm_{13}r_{015})] \| [r_{04}(1 + gm_4 r_{011})] \text{ --Eq. (24)}$$

The gain of the op-amp is then

$$A = \frac{V_0}{V_i} = g_m . R_0 \qquad \text{-----Eq. (25)}$$

The load capacitor C_L provides dominant pole compensation and the dominant pole will be at $\frac{1}{2\Pi R_0 C_L}$. The second stage M3, M4 introduces parasitic poles. These poles should be made larger than the unity gain frequency of the op-amp where $f_u = \frac{g_m}{2\Pi C_L}$. Using the values of gm and K from the model file, the W/L ratios of all the MOSFETs are evaluated.

4.1.1.1 Design procedure

For the required unity gain frequency f_u, the value of load capacitance C_L and required g_m value is decided. For differential pair M1M2 with current I, and using the expressions

$$gm = \sqrt{2\beta I_D} \qquad \text{-----Eq. (25)}$$

$$gm = \sqrt{2.K.\left(W/L\right)_{M1M2} I} \qquad \text{----- Eq. (26)}$$

We can evaluate $\left(W/L\right)$ of M1 and M2. Using M6 and R_{BIAS} and deciding the overdrive voltage for M6, we can make a current I to flow through RBIAS. M6, M5 combination is a current mirror. If equal currents of I are flowing through M1 and M2, then M5 must sink 2I. Therefore, using the current mirror action of M6 and M5, the $\left(\frac{W}{L}\right)_5$ must be made equal to $2\left(\frac{W}{L}\right)_6$. Using current mirror of M6, M9 combination and by adjusting $\left(\frac{W}{L}\right)_9$ with respect to $\left(\frac{W}{L}\right)_6$, we make appropriate current to flow through M9 and hence M8 and M7 to generate the required bias voltages. The current through M10 is sum of currents through M3 and M1. Based on the currents required in M1 and M3, the $\left(\frac{W}{L}\right)$ ratio of M10 and M3 are decided. Since, the current through M3 must be equal to the currents through M12 and M14, therefore $\left(\frac{W}{L}\right)$ ratio of M12 and M14 are decided. In a similar way, the current in M11 is shared by M2 and M4 and the current through M4 will flow through M13 and M15. This condition decides the $\left(\frac{W}{L}\right)$ ratio of M11, M4, M13 and M15. The M16, M17 combination is a source follower circuit and acts as a buffer to provide enough of load current. M16 sources the current to M17 and the load. Depending on the load current required $\left(\frac{W}{L}\right)$ ratio of M16 and M17 are decided.

The technology used is 0.18µm. To avoid Lambda effect, L must be at least two to five times the minimum value. Therefore, L = 0.5µm is used for all MOSFETs and then the widths are decided for the required $\left(\frac{W}{L}\right)$ ratios.

4.1.1.2 Simulation results

The simulation results are as shown in Fig. 11.

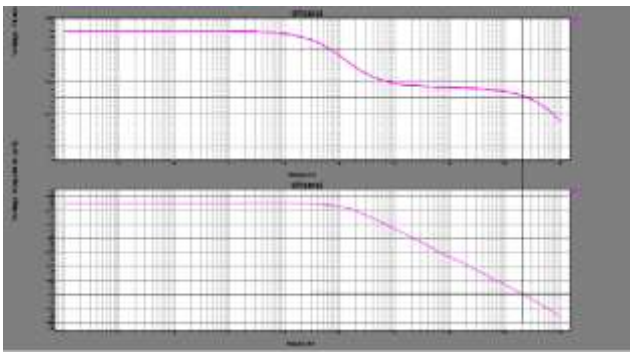

Fig. 11 Gain and phase Margin of Single ended Op-Amp

The simulation results show that the Op-Amp designed has an open loop gain of 65dB and a unity gain frequency of 200MHz at a phase margin of 78 degrees. The Op-Amp occupied an area of 332µm^2. The settling time of the op-amp in buffer mode is seen to be 7.2nS. The average power dissipation of this op-amp is 3.6mW.

4.1.2 Differential op-amp

The schematic of the implemented wide swing fully differential folded cascode op-amp is shown in Fig. 12. The circuit can be viewed as a combination of the folded cascode structure, the biasing circuit and the Common mode feedback circuit (CMFB) circuit. If input signal is applied to the NMOS differential pair M1 M2, it drives the cascode PMOS pair M7 M8 and hence the name folded cascode.

4.1.2.1 Design procedure

If the current through M5, M6 is 7.5µA, then, the $\left(\frac{W}{L}\right)$s of M1, M2 are adjusted to result in a current of 2.5µA through them (M1 and M2). Now M3 and M4 must handle 5µA. Also as 2.5µA of current is subtracted from M5, M6 current of 7.5µA, therefore the current through M7 to M12 transistors will be 5µA. The transistor M3, M9, M10 forms a current mirror and since all currents are 5µA, therefore W/L of M3, M9 and M10 will be equal. Similar is the case with the current mirror of M4, M11 and M12. The design procedure is similar to that discussed in section 4.1.1. The biasing circuit basically has two wide are swing current mirrors. The $\left(\frac{W}{L}\right)$ ratio of MB2 and MB9 are made ¼th of $\left(\frac{W}{L}\right)$ of other MOSFETs. The effective gate voltage considered here is 0.25V.

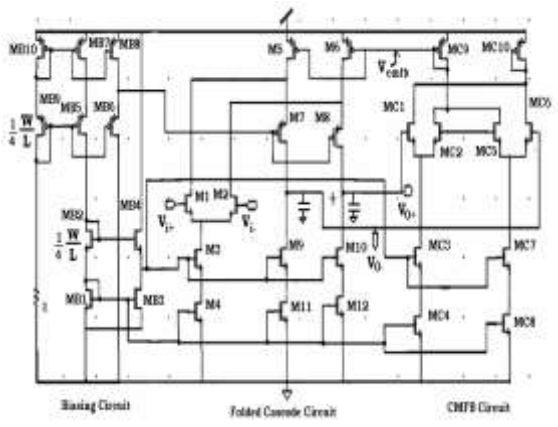

Fig. 12 Schematic of implemented Differential Op-Amp

The common mode feedback circuit is shown on the right side of Fig. 12. It consists of MOSFETs MC1 to MC10. This circuit rejects the differential signal and amplifies the common mode signal on its inputs. The differential outputs V_{0+} and V_{0-} of folded cascode structure are the inputs to this circuit. The output of this circuit is V_{CMFB}. If V_{0+} and V_{0-} are equal, then the output V_{CMFB} will be equal to a value required for M6 to result in the required 7.5µA. If $V_{0+} \neq V_{0-}$, then the differential pairs MC1, MC2 and MC5, MC6 amplifies the difference between the average of outputs and the common mode voltage i.e., $\frac{V_{0+}+V_{0-}}{2}$ and V_{CM}. Using this feedback, the circuit finally makes $\frac{V_{0+}+V_{0-}}{2}=V_{CM}$. If V_{0+} and V_{0-} increase above V_{CM}, then the drain currents of MC1 and MC6 will increase and hence currents through MC2, MC5 will decrease. This causes V_{CMFB} to increase. This increase in V_{CMFB} decreases the drain currents of M5, M6. This reduces V_{0+} and V_{0-} as currents through current sources M9 to M12 is constant. If V_{0+} and V_{0-} go below V_{CM}, then a similar, but opposite action is initiated and V_{CMFB} will make V_{0+} and V_{0-} to increase.

4.1.2.2 Simulation results

The simulation results of fully differential op-amp are shown in Fig. 4.4.

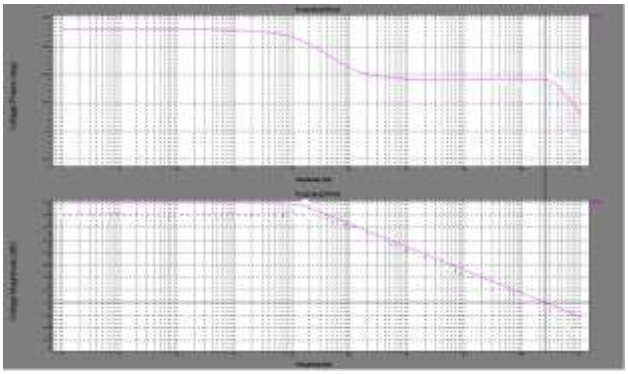

Fig. 4.4 Gain and phase Margin of Differential Op-Amp

The simulation results show that the Folded Cascode Differential Op-Amp designed has an open loop gain of 80dB and a unity gain frequency of 250MHz at a phase margin of 90 degrees. The Op-Amp occupied an area of 213µm². The settling time of the op-amp in buffer mode is seen to be 7.4nS. The average power dissipation of this op-amp is 3.5mW.

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