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# Sample and Hold Amplifiers for Pipelined A/D Converters

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The most crucial circuit in an A/D converter is the sample and hold circuit. During sampling mode, the input signal charges a capacitor and during hold mode, the charge on capacitor is held constant (until the next sampling) for the converter to complete conversion. This paper explains the implementation of S/H amplifier which works at 100 Mega samples /Sec. From the results it can be observed that peak output of 2V and occupies an area of 309μm$^2$. The minimum sampling time required is seen to be 8nS. The average power dissipation of this S/H amplifier is 3.83mW.

**Keywords:** Sample and Hold, Pipelined ADC, Switch capacitor, charge injection.

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ELECTRONICS RESEARCH ARTICLE

# Sample And Hold Amplifiers For Pipelined A/D Converters

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**ABSTRACT**

The most crucial circuit in an A/D converter is the sample and hold circuit. During sampling mode, the input signal charges a capacitor and during hold mode, the charge on capacitor is held constant (until the next sampling) for the converter to complete conversion. This paper explains the implementation of S/H amplifier which works at 100 Mega samples /Sec. From the results it can be observed that peak output of 2V and occupies an area of 309μm². The minimum sampling time required is seen to be 8nS. The average power dissipation of this S/H amplifier is 3.83mW.

**Keywords:** Sample and Hold, Pipelined ADC, Switch capacitor, charge injection

## 1. INTRODUCTION

*SAMPLE AND HOLD CIRCUITS*

Ideally, an S/H circuit must have an output waveform as shown in Fig. 1(a). During sampling, the analog input may vary and hence the need for another circuit called track and hold circuit. Here during sampling, the analog input is tracked and the value is maintained during hold mode as shown in Fig. 1 (b).

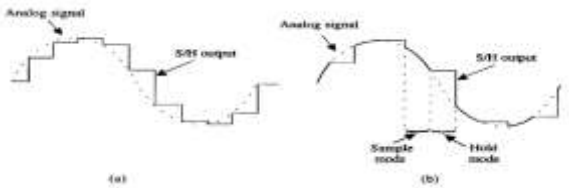


Fig. 1 Output of an ideal (a) S/H circuit and (b) Track and Hold

Fig. 2shows the major errors that can result in S/H circuit. The time required for the S/H circuit to track the input signal within tolerable limits is called "Acquisition time". If amplifier is undercompensated (phase margin <900) then an overshoot occurs and op-amp takes some time to settle within ± ½ LSB. This is called "Settling Time". During hold mode, the pedestal error results due to charge injection and clock feed through. The charge leakage from capacitor results in droop.

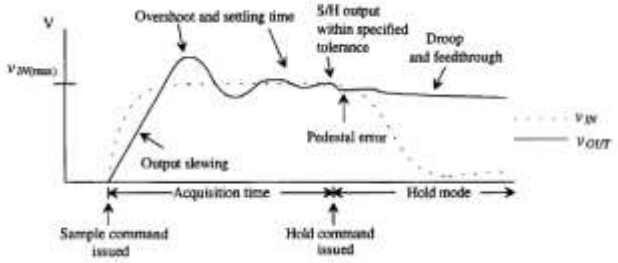


Fig. 2 Errors associated with S/H circuit

1.1 Basic S/H circuit

The simplest form of S/H circuit is shown in Fig. 3.

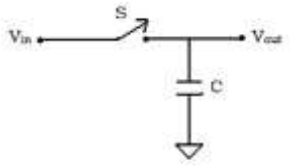


Fig. 3. Basic S/H circuit

During sampling, switch S is closed and the input is sampled onto capacitor C. During hold mode S is opened, so that the capacitor retains the value. The small signal bandwidth for the circuit is decided by the capacitor C and the ON resistance (RON) of the switch.

$$f_{3dB} = \frac{1}{2\Pi R_{ON} C} \qquad \text{----- Eq. (1)}$$

### 1.2 S/H circuit with input and output buffers

To avoid loading onto the source input and output buffers can be added as shown in Fig. 4. [1] [2].

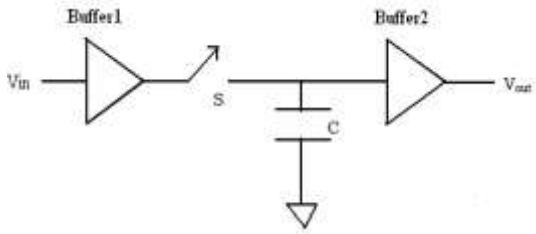


Fig. 4 S/H circuit with input and output buffers

If the source current is $I_{in}$, the slew rate of the S/H circuit is given by

$$\frac{dV}{dt} = \frac{I_{in}}{C} \qquad \text{----- Eq. (2)}$$

For better slewing, $I_{in}$ must be large and this is provided by the input buffer. The overall accuracy is dictated by the op-amps used in buffer.

### 1.3 Switched Capacitor S/H circuit

The sample and hold circuit using switched capacitor is shown in Fig. 5.

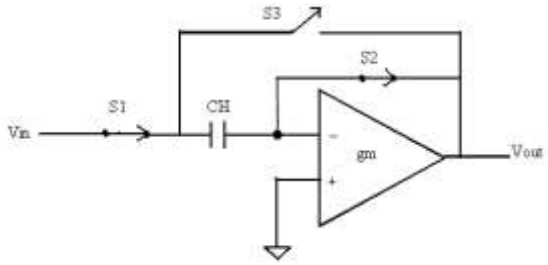


Fig. 5. Switched Capacitor S/H circuit

The switch positions shown in Fig. 5 are for sampling mode. All the switches change their positions during hold mode. The circuit functionality is similar to Fig. 4. The switches must be carefully designed. Otherwise, they introduce charge feed through and aperture uncertainties. The S/H circuits with gain can also be implemented using switched capacitor circuits and is shown in Fig. 6. The circuit has three switches S1 to S3 and two capacitors $C_i$ and $C_f$. Fig. 6.shows the circuit in sampling mode. During sampling phase, the input is sampled onto $C_f$ and $C_i$ and the op-amp works like a buffer. The switches change their positions during hold mode so that $C_i$ is connected between ground and input of op-amp while $C_f$ is connected in the feedback path of the op-amp. Now the op-amp works like an inverting amplifier with a gain of $(1+C_i/C_f)$. If $C_i = C_f$ then a gain of two is achieved.

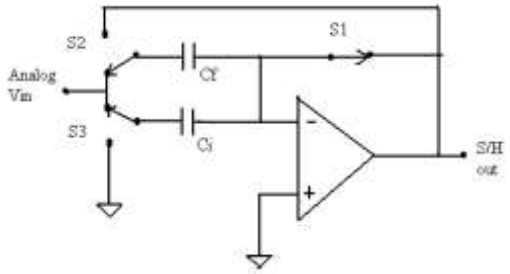


Fig.6. Switched capacitor S/H circuit with gain

The accuracy of this circuit is decided by the ratio of capacitances. The offset errors and common mode noise can be effectively removed if differential S/H circuits are used as shown in Fig. 7.

At $t=t_0$, S1 and S2 are closed while S3 is opened. The analog input is now sampled onto capacitors. At $t=t_1$, S1 opens while S2 is still closed. Now the op-amp is in open loop mode. As the top plate of 'C' is at ground, the capacitive feedthrough and charge injection because of S1 going OFF becomes independent of input signal. At $t=t_2$, when S2 goes OFF, the charge injection flows into the V+ and V- and not onto capacitors as op-amp input impedance is very high. Therefore, the sampled charge on capacitor is unaffected. This sequence of turning OFF of switches is called "Bottom plate sampling" [3].

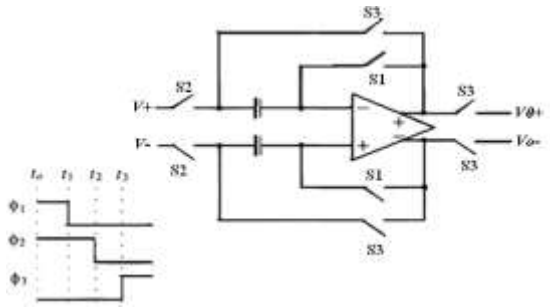


Fig. 7 Fully differential sample and hold circuit

At t=t3, the circuit goes into hold mode, with op-amp again in closed loop configuration and acts as a buffer to hold the value of capacitor. By adding additional capacitors and switches, we can realize fully differential S/H circuit with gain.

## 2. ERROR SOURCES IN S/H CIRCUITS

The likely deviations in S/H circuit output are shown in Fig. 2 and the sources for these errors [4] [5] could be switch errors, kT/C noise, charge injection and capacitive feed through.

### 2.1 kT /C Noise:

The output RMS noise of a simple RC circuit is equal to . This can be treated as equal to a voltage sampled onto a capacitor through an ON switch with a resistance R [6]. Substituting the values of k and T we see that the RMS noise equals 64μV for a capacitor C of 1pF and increases to 200μV for 0.1pF. Therefore, larger the capacitance value, smaller is the RMS noise. But for high speeds, the capacitor value must be small to result in fast charging/discharging. Therefore a tradeoff is to be made between high speed and low noise. The dynamic power consumption is also seen to be proportional to C. Therefore, a careful selection of the value of 'C' is to be made.

### 2.2 Switch errors:

The various switch configurations and their characteristics are shown in Fig. 8. If NMOS transistor is used as a switch, the maximum voltage it can pass is (VDD-VthN) and if a PMOS is used as switch, then the lowest voltage it can pass is VthP.

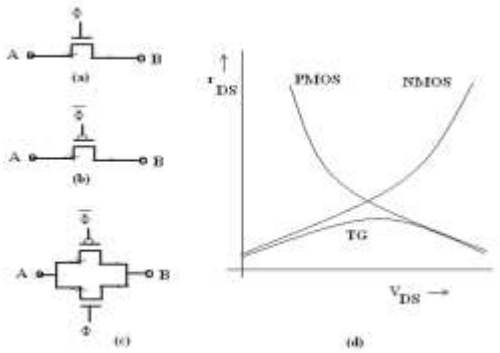


Fig. 8. (a) NMOS switch (b) PMOS switch
(c) CMOS transmission gate
(d) Characteristics of switches

If CMOS transmission gate is used as a switch, it can pass a logic high or logic low without any threshold drop. The non-idealities associated with these switches limits their usage for some applications like switched capacitor circuits [7]. The two well-known non-idealities are charge injection and clock feed through.

### 2.3 Charge injection

The principle of charge injection can be explained with Fig. 9.

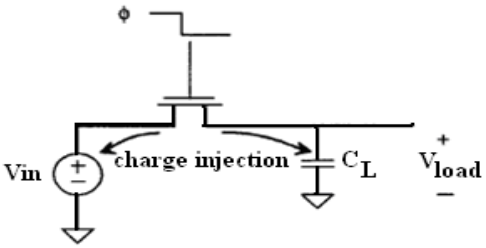


Fig. 9. NMOS switch illustrating charge injection

When the MOSFET is ON, a charge Qch' is built into the channel and when the MOSFET is made OFF, this charge is injected on both sides into Vs and also the load capacitance CL. Since Vs is of low impedance, the injected charge will not have much effect. However, the injected charge onto CL results in a change in voltage across it. The charge/unit area induced in the channel is

$$Q'_{ch} = C_{ox}(V_{GS} - V_{tn}) \quad \text{----- Eq. (3)}$$

Then, the total charge in the channel is

$$Q_{ch} = C_{ox.}W.L(V_{GS} - V_{tn}) \quad \text{----- Eq. (4)}$$

If the clock signal on the gate turns OFF fast, then this charge distributes equally on either sides of the

switch [8]-[10]. Therefore, the change in voltage across $C_L$ is

$$\Delta V_L = -\frac{C_{ox}.W.L(V_{GS}-V_{tn})}{2C_L} = -\frac{C_{ox}.W.L(V_{DD}-V_{in}-V_{tn})}{2C_L} \quad \text{---- Eq. (5)}$$

The change in voltage across load is nonlinear since $V_t$ is in the equation and hence results in non-linearity error in S/H circuits.

### 2.4 Capacitive feedthrough

The capacitances between Gate-Source and Gate-Drain are shown in Fig. 10. When Gate input goes high, the clock signal feeds through the Gate-Source capacitance and Gate-Drain capacitances. Also, since MOSFET is ON, $V_{in}$ is also connected to $C_L$. Therefore, $C_L$ is charged to $V_{in}$ and capacitance feedthrough will not have any effect [8]-[10].

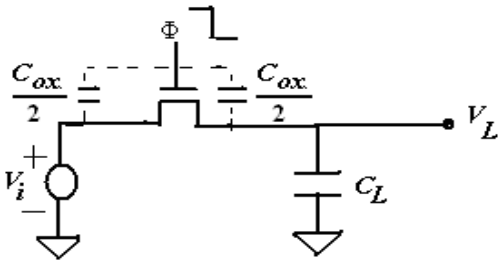


Fig.10 Illustration of capacitive feedthrough

When Gate input goes low, MOSFET is OFF and portion of clock signal appears across $C_L$ given by

$$\Delta V_L = \frac{C_{gd}(V_{DD}-V_{ss})}{C_{gd}+C_L} \quad \text{---- Eq. (6)}$$

Where $C_{gd}$ is the overlap capacitance formed by the overlap of Gate and Drain areas and is given by

$$C_{gd} = C_{ox}.W.LD \quad \text{----- Eq. (7)}$$

Where LD is overlap area of Gate/Drain or Gate/Source.

### 2.5 Minimization of charge injection and clock feedthrough

One of the most widely used techniques to reduce the errors due to switch non-identities is to use a dummy switch [10] [11] as shown in Fig. 11. Here, we add another MOSFET switch M2, whose Drain and Source are shorted and the (W/L) of this dummy switch must be ½ (W/L) of the other MOSFET M1. The two MOSFETs are driven by alternate clock phases. When M1 goes OFF, half of the channel charge is injected towards the dummy switch.

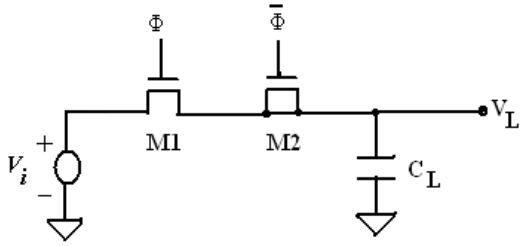


Fig. 11 Dummy switch used to minimize charge injection

Even though drain and source of M2 is shorted, it can still induce a charge. Therefore the charge injected by M1 is stored in channel M2 and hence doesn't change the charge on CL. When M2 goes OFF, M1 is ON and the charge in M2 goes towards low impedance Vi and not onto $C_L$. Using transmission gates also reduces charge injection but the complementary clocks on PMOS and NMOS gates must be precisely controlled. Another method is to use fully differential circuits to cancel these effects as these non-idealities appear as common mode signal to the amplifier.

## 3. IMPLEMENTING THE S/H AMPLIFIER

The implemented schematic of S/H amplifier is shown in Fig. 12. The differential op-amp is used here. During sampling i.e., during t0 to t1, the Φ1 and Φ2 switches are closed. The input voltage Vi is sampled and stored onto the capacitors. During this duration the op-amp is in closed loop and acts like buffer.

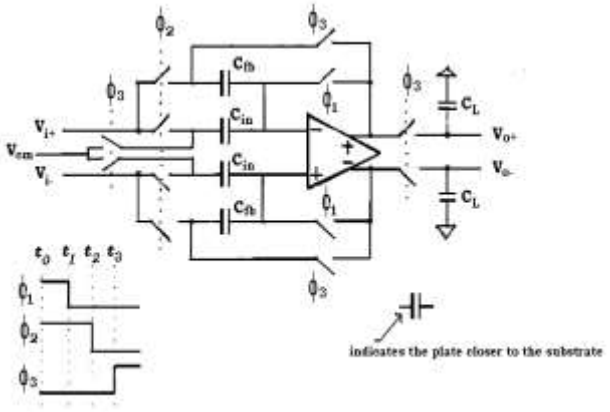


Fig. 12 Fully Differential Sample and Hold circuit

During $t_1$ to $t_2$, the op-amp is in open loop and between $t_2$ to $t_3$ all the switches are open. This sequence of switching is called bottom plate sampling. When $\Phi_3$ switches are closed, the op-amp works like an amplifier with a gain of $\left(1+\frac{C_{in}}{C_{fb}}\right)$. The input-output relationship of this circuit is evaluated as follows. When $\Phi_1$ and $\Phi_2$ switches are closed and $\Phi 3$ is open the charge stored on $C_{in}$ and $C_{fb}$ is

$$Q_{in,fb} = C_{in,fb}(V_i - V_{cm} \pm V_{offset}) \text{ ----- Eq. (8)}$$

Where $V_{offset}$ is the offset voltage of the op-amp used. When $\Phi_3$ is closed, the net charge on $C_{in}$ will be

$$Q_{in} = C_{in}(V_{cm} - V_{cm} \pm V_{offset}) \text{ ----- Eq. (9)}$$

The difference in voltages on $C_{in}$ between $\Phi_1$ and $\Phi_3$ will be transferred to $C_{fb}$. Using charge conservation principle, we get

$$C_{fb}(V_0 - V_{cm} \pm V_{offset}) = C_{in}(V_i - V_{cm} \pm V_{offset}) + C_{fb}(V_i - V_{cm} \pm V_{offset}) - C_{in}(V_{cm} - V_{cm} \pm V_{offset}) \text{--Eq. (10)}$$

Therefore,
$$V_0 = V_i\left(1+\frac{C_{in}}{C_{fb}}\right) - \frac{C_{in}}{C_{fb}}V_{cm} \quad \text{Eq. (11)}$$

indicates that the offset voltages are cancelled out. For fully differential inputs and outputs, Eq. (11) can be written as

$$V_0 = (V_{0+} - V_{0-}) = \left(1+\frac{C_{in}}{C_{fb}}\right)(V_{i+} - V_{i-}) \text{ ----- Eq. (12)}$$

Eq. (12) indicates that the common mode voltage is removed by the differential op-amp configuration.

### 3.1 Implementing subtraction in S/H

In individual stages of pipeline ADCs, the residue of a stage must be provided with a gain. For this, the S/H circuit needs to subtract two input signals and amplify the residue. This functionality can be implemented by removing $V_{cm}$ from Fig. 12 and replacing it by the two signals $V_{di+}$ and $V_{di-}$ coming from the DAC [12]. The circuit is shown in Fig. 13.

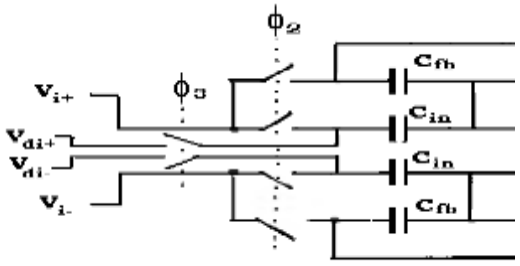


Fig. 13 Fully Differential S/H circuit implementing subtraction

As per the previous analysis, when $\Phi_3$ is closed, the charge $C_{in}$ will be

$$Q_i = C_{in}(V_{di+} - V_{cm} \pm V_{offset}) \text{ ----- Eq. (13)}$$

$$V_{0+} = \left(1+\frac{C_{in}}{C_{fb}}\right)V_{i+} - \frac{C_{in}}{C_{fb}}V_{di+} \text{ ----- Eq. (14)}$$

For differential input and output Eq. (14) modifies to

$$V_0 = (V_{0+} - V_{0-}) = (V_{i+} - V_{i-})\left(1+\frac{C_{in}}{C_{fb}}\right) - \frac{C_{in}}{C_{fb}}(V_{di+} - V_{di-}) \text{ ----- Eq. (15)}$$

If $C_{in}$ = $C_{fb}$, we get a gain of 2 and by properly adjusting the ratio of, we can get different gains. Here, all the switches are realized using CMOS transmission gates. The implemented schematic is shown in Fig. 4.9.

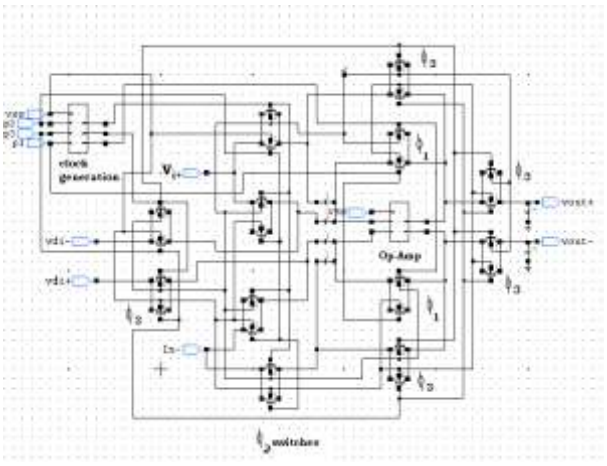


Fig. 14 Schematic of implemented S/H circuit

#### 4.3.2 Simulation results

The simulation results of the implemented S/H amplifier are shown in Fig. 15. The simulation results show the sample and hold circuit working at 100

Mega samples /Sec. The differential input signals are of ±0.5V. The S/H amplifier output is expected to be $2(V_{i+} - V_{i-})$ which is 2V.The simulation results also show a peak output of 2V. Hence the functionality is verified. The S/H amplifier occupied an area of 309μm2. The minimum sampling time required is seen to be 8nS. The average power dissipation of this S/H amplifier is 3.83mW.

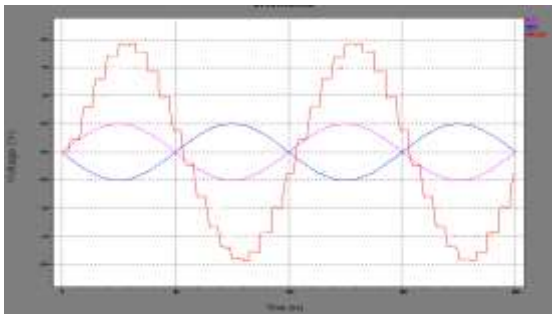

Fig. 15 Simulation results of S/H circuit

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