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Research Article

Sample and Hold Amplifiers for Pipelined A/D Converters

Dr. P. Prasad Rao

Corresponding Author:
prasadrao_hod@yahoo.co.in

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ABSTRACT

The most crucial circuit in an A/D converter is the sample and hold circuit. During sampling mode, the input signal charges a capacitor and during hold mode, the charge on capacitor is held constant (until the next sampling) for the converter to complete conversion. This paper explains the implementation of S/H amplifier which works at 100 Mega samples /Sec. From the results it can be observed that peak output of 2V and occupies an area of 309μm^2. The minimum sampling time required is seen to be 8nS. The average power dissipation of this S/H amplifier is 3.83mW.

Keywords: Sample and Hold, Pipelined ADC, Switch capacitor, charge injection.

Professor, Dept. of ECE,
Vaagdevi College Engineering, Affiliated to JNTUH, Warangal-506005.

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